Digital Totem Pole PFC Controller with I2C & UART Interfaces

HP1010A

FEATURES

- Highly flexible digital Totem Pole PFC controller
- High flexibility digital PWM
  - PWM frequency ranges from 20 kHz to 200 kHz
  - PWM soft start during AC line zero-crossing
  - Switching frequency spread spectrum for improved EMI
- High performance control loop
  - 25 MHz sigma-delta ADC for line voltage and current sense, 12.5 MHz sigma-delta ADC for output voltage
  - Enhanced dynamic loop response
  - Input voltage feedforward to avoid reverse current during AC drop
  - Control loop parameters can be configured separately for operating modes and input voltage
  - Support HVDC input
- Multi−mode operations
  - Continuous Conduction Mode (CCM) in heavy load Conditions
  - Discontinuous Conduction Mode (DCM) in light load conditions
  - Burst mode in the zero load conditions
  - The mode parameters can be configured separately for high line and low line
- Advanced control functions
  - True RMS power metering
  - Inrush current control with programming relay delay
  - Output voltage follows power variation
  - Relay power-saving mode
  - PFC quick start function
- Extensive fault protections
  - Fast over-voltage protection
  - Bulk under-voltage protection and over-voltage protection
  - External NTC thermal protection
  - Cycle−by−cycle current limit
  - Average switching current protection
- Built-in 128 bytes MTP to store custom configurations
- I²C and UART interfaces
- Programming via easy-to-use Graphical User Interface (GUI)
- Available in QFN4×4-24L packages
- -40°C to 125°C operating temperature

APPLICATIONS

Ultra−High Efficiency Power Supplies
LED Lighting
Industrial Power Supplies
Server/Telecom
EV/E-Bike Charger
Supercomputing
Variable-Frequency Drivers (VFD)

GENERAL DESCRIPTION

The HP1010A is a highly flexible digital Power Factor Correction (PFC) controller designed to drive a totem pole PFC power stage.

Totem-pole PFC is composed of a fast-leg using the third-generation semiconductor (GaN or SiC MOSFET) switching at PWM frequency and a slow-leg operating at the AC frequency. This design allows for a considerable increase in efficiency and power density by removing the diode bridge that is present at the input of a traditional PFC circuit.

The HP1010A offers RMS values of input voltage, current, and power. Through the I²C and UART interfaces, this information can be communicated to a microcontroller.

The HP1010A operates from a single 3.3 V supply. The device is available in a 4 mm x 4 mm QFN4×4-24L package specified over an ambient temperature range of −40°C to +125°C.

TYPICAL APPLICATION CIRCUIT

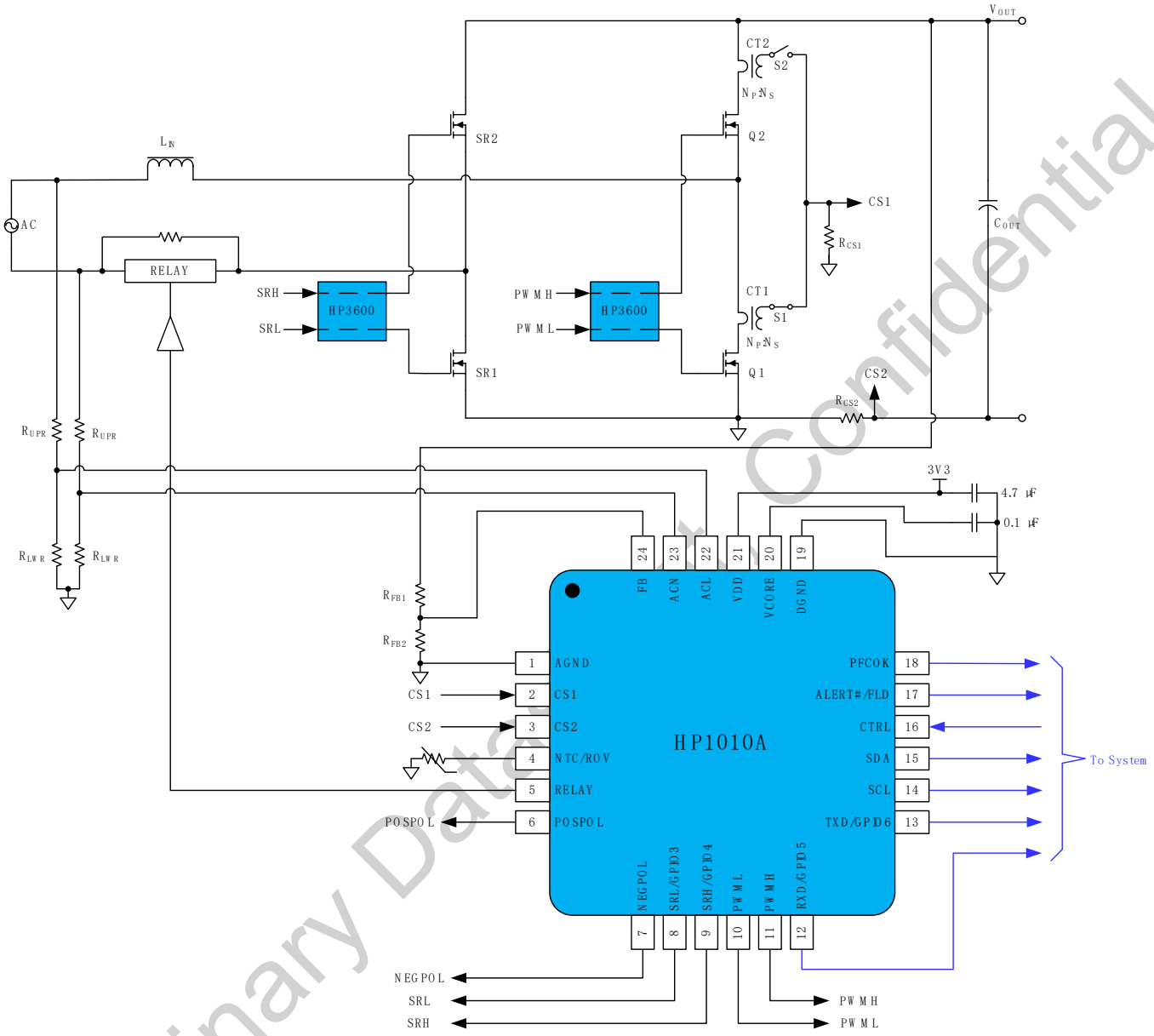

Figure 1 Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	11/2025	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

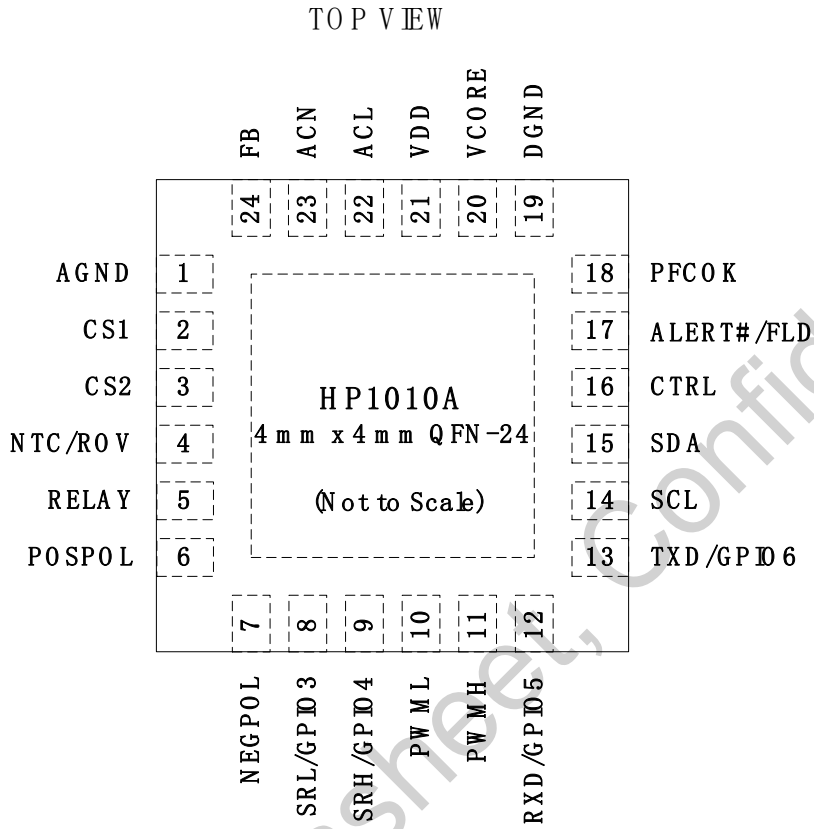


Figure 2 HP1010A-AA000-QN24R Pin Assignment

Table 1. Pin Function Descriptions for HP1010A-AA000-QN24R

Pin No.	Name	Type[1]	Description
1	AGND	P	**Analog Ground.** AGND should be connected directly to DGND.
2	CS1	AI	**CS1 Sense.** This pin senses the inductor current upslope through current sense transformers in the TPPFC topology. It is used to reconstruct the inductor current. It is also used for cycle−by−cycle current limiting. The signal is referred to AGND.
3	CS2	AI	**CS2 Sense.** This pin optionally senses the inductor current downslope. The signal is referred to AGND.
4	NTC/ROV	AI	**Dual Function Pin.** NTC: Temperature sense input, which is inverse proportional to the temperature, triggers the comparator when OTP happens. ROV: redundant OVP comparator with a programmable reference. The signal is referred to AGND.
5	RELAY	DO	**Relay Control Output.** The turn-on delay can be programmed. The signal is referred to DGND.
6	POSPOL	DO	**Positive Polarity of AC Input.** Positive Output of the internal AC polarity detection circuit. The signal is referred to DGND.
7	NEGPOL	DO	**Negative Polarity of AC Input.** Negative output of the internal AC polarity detection circuit. The signal is referred to DGND.
8	SRL/GPIO3	DO	**PWM Output for Low Side of Slow Leg.** The signal is referred to DGND. It can be re-used as GPIO pin.
9	SRH/GPIO4	DO	**PWM Output for High Side of Slow Leg.** The signal is referred to DGND. It can be re-used as GPIO pin.
10	PWML	DO	**PWM Output for Low Side of Fast Leg.** The signal is referred to DGND.

Pin No.	Name	Type[1]	Description
11	PWMH	DO	**PWM Output for High Side of Fast Leg.** The signal is referred to DGND.
12	RXD/GPIO5	DIO	**UART_RX Pin.** UART Receive Data pin. The signal is referred to DGND. It can be re-used as GPIO pin.
13	TXD/GPIO6	DIO	**UART_TX Pin.** UART Transmit Data pin. The signal is referred to DGND. It can be re-used as GPIO pin.
14	SCL	AIO	**I²C Serial Clock Line.** The SCL signal is referred to DGND.
15	SDA	AIO	**I²C Serial Data Line.** The SDA signal is referred to DGND.
16	CTRL	DI	**Remote Control Pin.** The signal is referred to DGND.
17	ALERT#/FLD	DIO	**I²C Alert Pin.** The signal is referred to DGND. It can be re-used as fast-load transition detection.
18	PFCOK	DIO	**PFCOK Indicates Pin.** The PFCOK function is held low when the PFC output voltage is out of regulation and during fault conditions. It is a push−pull output.
19	DGND	P	**Digital Ground.** DGND should be connected directly to AGND.
20	VCORE	P	**1.8 V VDD for Digital Core.** The VCORE signal is referred to DGND. Connect a 100 nF capacitor from VCORE to DGND.
21	VDD	P	**3.3 V Main Supply.** The VDD signal is referred to AGND. Connect a 4.7 μF capacitor from VDD to AGND.
22	ACL	AI	**AC Line Voltage Sense.** The signal is referred to AGND.
23	ACN	AI	**AC Neutral Voltage Sense.** The signal is referred to AGND.
24	FB	AI	**PFC Output Voltage Sense.** The signal is referred to AGND.

[1] Legend:

A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Operating Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3	3.3	3.6	V
Supply Current	I_{DD}	Normal operation		10.0		mA
		V_{DD} = 3.3 V while programming			7.5	mA
Shutdown Current	I_{DD_SD}	PFC off state		8.1		mA
Sleep Mode Current	I_{DD_SM}	Sleep mode enabled.		1.0		mA
POWER-ON RESET						
Power-on Reset	V_{DD_POR}	V_{DD} rising	2.7	2.8	2.9	V
UVLO	V_{DD_UVLO}	V_{DD} falling	2.55	2.65	2.75	V
VCORE PIN						
Output Voltage	V_{CORE}	100 nF capacitor connected to DGND	1.7	1.8	1.9	V
OSCILLATOR, CLOCK, PLL						
Oscillator Frequency	f_{OSC}			12.5		MHz
PLL Frequency	f_{PLL}			200		MHz
Digital PWM Resolution	t_{PWM_RES}	For PWML and PWMH pins		5		ns
PWMH, PWML, SRH, SRL, POSPOL, NEGPOL, RELAY PINS						
Output Low Voltage	V_{PWMOL}	Sink current = 10 mA			0.4	V
Output High Voltage	V_{PWMOH}	Source current = 10 mA	V_{DD} - 0.4			V
Rise time	t_{RISE}	V_{DD} = 3.3 V, C_{LOAD} = 50 pF 10%V_{DD} to 90%V_{DD}		25		ns
Fall time	t_{FALL}	V_{DD} = 3.3 V, C_{LOAD} = 50 pF 90% V_{DD} to 10%V_{DD}		25		ns
Output Source Current	I_{OL}	V_{DD} = 3.3 V	-10			mA
Output Sink Current	I_{OH}	V_{DD} = 3.3 V			10	mA
SWITCHING FREQUENCY						
Frequency Range	f_{SW}		20		195	kHz
Accuracy			-3		3	%
ACN AND ACL PINS						
Input Impedance				78		kΩ
Input Voltage Range	V_{AC}		0		2.8	V
Amplifier Gain	G_{AC_OP}			0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Data updating frequency 25 kHz		12		Bits
Voltage Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-2.0		2.0	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUX Positive Comparator						
Threshold Range			40		340	mV
Threshold Accuracy		Test at 200 mV threshold	-30		30	
Resolution				4		Bit
LSB				20		mV
Hysteresis				40		mV
Propagation Delay					1.0	μs
AUX Negative Comparator						
Threshold Range			40		340	mV
Threshold Accuracy		Test at 200 mV threshold	-30		30	
Resolution				4		Bit
LSB				20		mV
Hysteresis				40		mV
Propagation Delay					1.0	μs
AC Line Frequency Monitor						
High Threshold	f_{5060_H}		68	70	72	Hz
Lower Threshold	f_{5060_L}		37	40	43	Hz
Detection Timer	N_{LINE_DET}		0.5		2	cycles
Exceed Timer	$N_{LINE\_FREQ\_EXC}$			2		cycles
Brown-out and SAG						
Vin On Threshold	V_{IN_ON}	Programmable, $K_{AC\_DIV\_EXT}$ = 1/200	0	78	255	VAC
Vin Off Threshold	V_{IN_OFF}	Programmable, $K_{AC\_DIV\_EXT}$ = 1/200	0	71	255	VAC
Brown-out Debounce	t_{BO_DEB}		-	0.5	-	cycles
Line Sag Timeout Range	t_{SAG_TO}	Programmable 4 to 32 AC cycles	4	12	32	cycles
High/Low Line Detection						
High Threshold	V_{HLINE}	Programmable, $K_{AC\_DIV\_EXT}$ = 1/200	120	168	180	VAC
Low Threshold	V_{LLINE}	Programmable, $K_{AC\_DIV\_EXT}$ = 1/200	120	156	180	VAC
High Line to Low Line Debounce Time	t_{H2L_DED}			1		cycles
VAC ZERO CROSSING DETECTION						
VAC Zero Detection Comparator		Between ACL pin to ACN pin				
Threshold	V_{POL_DET}		-10	0	10	mV
Hysteresis Width	V_{POL_HYS}			10		mV
Propagation Delay	t_{POL_PD}				1.0	μs
Digital Polarity Detection						
Digital Propagation Delay				5		μs
VIN_POL Detection Debounce	t_{POL_DEB}		5		80	μs
VIN_POL Detection LSB				5		μs
Main PWM Drive Control						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Main PWM On Threshold	V_{PWM_ON}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	V
Main PWM Off Threshold	V_{PWM_OFF}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	
SYNC PWM Drive Control						
SYNC On Threshold	V_{SYN_ON}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	
SYNC Off Threshold	V_{SYN_OFF}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	
Slow Leg (SR) Drive Control						
SR On Threshold	V_{SR_ON}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	
SR Off Threshold	V_{SR_OFF}	Low-line mode	0		32.8	V
		High-line mode	0		65.6	
SYNC PWM Drive Control 2						
SYNC On Threshold	$I_{SYN\_ON\_CS}$	Low-line mode	0.1		1.75	A
		High-line mode	0.2		3.5	A
SYNC Off Threshold	$I_{SYN\_OFF\_CS}$	Low-line mode	0.1		1.75	A
		High-line mode	0.2		3.5	A
Slow Leg (SR) Drive Control 2						
SR On Threshold	I_{SRON_CS}	Low-line mode	0.1		1.75	A
		High-line mode	0.2		3.5	A
SR Off Threshold	I_{SROFF_CS}	Low-line mode	0.1		1.75	A
		High-line mode	0.2		3.5	A
FB PIN						
Input Voltage			0		2.8	V
Input Impedance				350		kΩ
Amplifier Gain				0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				12.5		MHz
Equivalent Resolution				11		Bits
Voltage Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-1		1	%
Fast Over-Voltage Protection						
Threshold Range	$V_{FB\_FOV\_LIM}$		1.9		2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-1.5		1.5	%
Resolution				6		Bits
Hysteresis				100		mV
Propagation Delay	$t_{FB\_FOV\_PD}$				160	ns
Debounce Time	$t_{FB\_FOV\_DB}$	Programmable in 4 steps	40		100	µs
Blanking time	$t_{FB\_FOV\_BK}$			10		µs
Open Loop Protection						
Sink Current	I_{FB_SNK}			250		nA
Threshold	V_{FB_OL}		2		70	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution				4		Bits
Hysteresis	V_{FB_OLHYS}			18		V
Debounce Time	t_{FB_OLDB}	Programmable in 4 steps	1		4	cycles
Slow Over-Voltage Protection						
Threshold	$V_{FB\_SOV\_LIM}$		V_{REF}		V_{REF} + 68	V
Resolution				5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SOV\_DB}$		0		0.48	ms
Slow Under-Voltage Protection						
Threshold			V_{REF} - 68		V_{REF}	V
Resolution	$V_{FB\_SUV\_LIM}$			5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SUV\_DB}$		0		30	ms
CS1 AND CS2 PINS						
Input Voltage			0		1.4	V
Input Impedance				160		kΩ
Amplifier Gain				1		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Updating frequency at 100 kHz		8		Bits
Current Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-1.5		1.5	%
CS1 Fast Over Current Protection						
Threshold Range	$V_{CS1\_OC\_LIM}$		1.0		1.5	V
Threshold Accuracy		Factory trimmed at 1.25 V	-1.2		0.48	%
Resolution				6		Bits
LSB				7.8		mV
Hysteresis				25		mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	480		1920	ns
Debounce Time		Programmable in 4 steps	80		200	ns
CS2 OCP Detection						
Threshold Range	V_{CS2_OCP}		50		237	mV
Threshold Accuracy		Factory trimmed at 150 mV	-15		15	mV
Resolution				4		Bits
LSB				12.5		mV
Hysteresis				25		mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	80		640	ns
Debounce Time		Programmable in 4 steps	80		600	ns
CS2 Zero Crossing Detection						
Threshold Range	V_{CS2_ZCD}		7.6		68	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Threshold Accuracy		Factory trimmed at 38 mV	-4		4	mV
Resolution				6		Bits
LSB				0.95		mV
Hysteresis				15		mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	80		640	ns
Debounce Time		Programmable in 4 steps	80		600	ns
CTRL PIN						
Input Low Voltage	V_{CTRL_IL}				0.8	V
Input High Voltage	V_{CTRL_IH}		2.0			V
Debounce Time	t_{CTRL_DEB}			10		µs
Leakage Current	i_{CTRL_LK}				1.0	µA
PFCOK PINS						
Output Low Level					0.8	V
Output High Level			2.0			V
Debounce Time			0		200	ms
OVER AVERAGE SWITCHING CURRENT PROTECTION						
Average OCP Threshold		CS1 sense ratio is 10:1	0		14	A
Resolution				7		Bits
Accuracy			-2		+2	%
Debounce				2		Switch cycle
NTC/ROV PIN						
Current Source	I_{NTC}		43	46	49	µA
Over-temperature Threshold	V_{NTC_OT}		0.36	0.4	0.41	V
OT Recover Threshold	V_{NTC_REC}		0.78	0.8	0.82	V
Debounce Time	t_{NTC_DEB}	Programmable in 2 steps		500	1000	ms
Redundant Over-Voltage Protection						
Threshold Range	V_{ROV_LIM}		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-2.00		1.64	%
Resolution				6		Bits
Hysteresis				100		mV
Propagation Delay					160	ns
Debouncing Time		Programmable in 4 steps	40		100	µs
Blanking Time				10		µs
SDA/SCL PINS						
Input Voltage Low					0.8	V
Input Voltage High			2.2			V
Output Voltage Low					0.4	V
Pull-Up Current			100		350	µA
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock Frequency	f_{IIC}				400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			µs
Start Setup Time	t_{SU_STA}		4.7			µs
Start Hold Time	t_{HD_STA}		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_{R_I2C}				1000	ns
SCL, SDA Fall Time	t_{F_I2C}				300	ns
Data Setup Time	t_{SU_DAT}		250			ns
Data Hold Time	t_{HD_DAT}		300			ns
TXD/RXD PINS (UART)						
Baud Rate	f_{UART}	Programmable with (0: 9600; 1: 1200; 2: 57600; 3: 115200)	1200	9600	115200	bps
Data Length				8		
Stop Bits				1		
Polarity Check Bit				1		
EEPROM RELIABILITY						
Endurance		T_A = 85°C	10000			Cycles
		T_A = 125°C	1000			Cycles
Data Retention		T_A = 85°C	20			Years
		T_A = 125°C	15			Years

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute maximum ratings

Parameter	Rating
VDD (Continuous)	4.2 V
ACL, ACN, FB, CS1, CS2, RELAY, NTC/ROV, POSPOL, NEGPOL, SRL/GPIO3, SRH/GPIO4, PWML, PWMH, RXD/GPIO5, TXD/GPIO6, SCL, SDA, CTRL, ALERT#/FLD, PFCOK	-0.3 V to V_{DD} + 0.3 V
VCORE	2 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	±6000 V
Charge Device Model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN4x4-24L	46	23	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

OPERATING PRINCIPLE OF TOTEM-POLE PFC

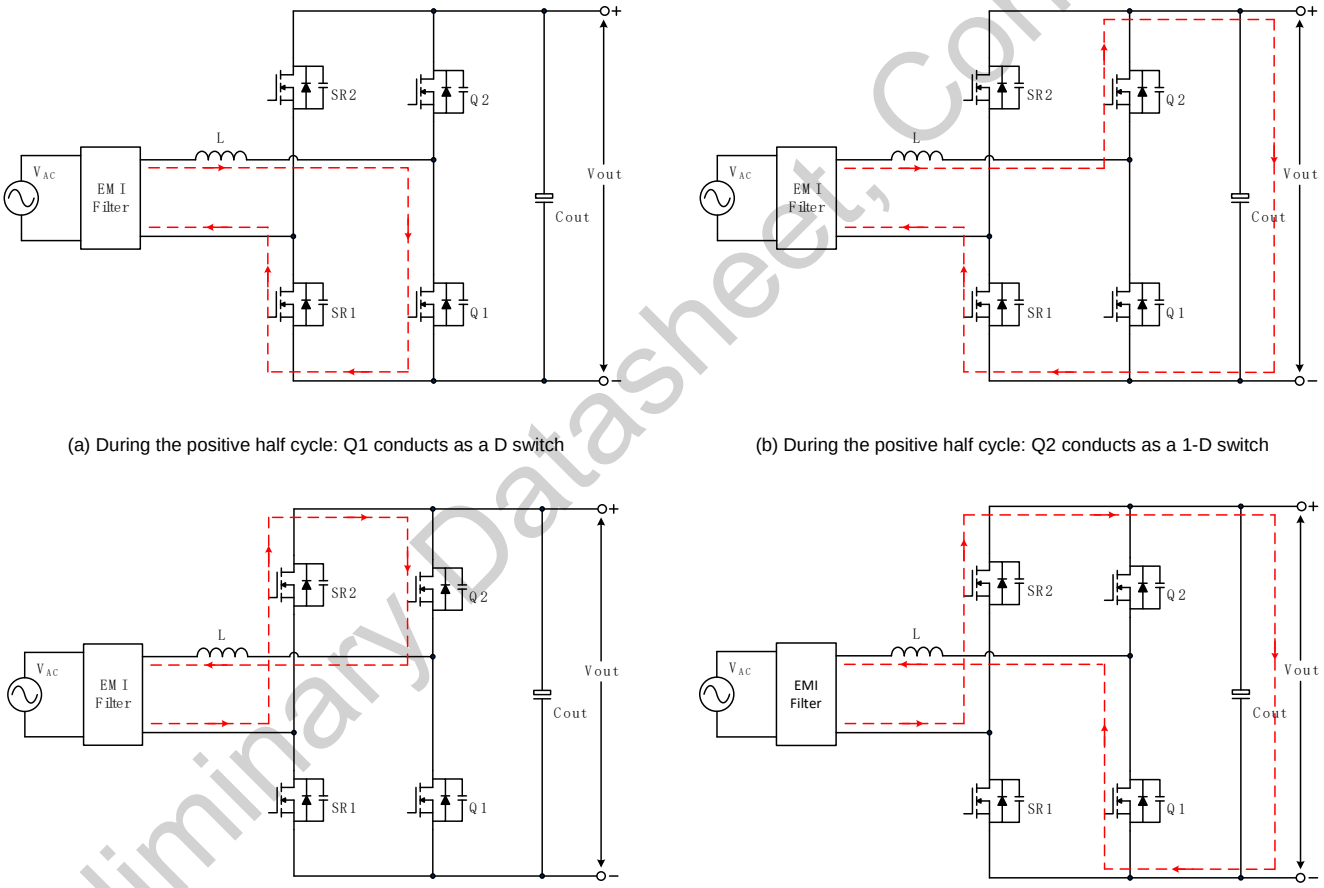
The working principle of the totem-pole PFC is illustrated in Figure 3.

During the positive half-cycle of the input voltage, the slow leg SR1 conducts. When the fast leg lower switch Q1 operates as a D switch, the inductor magnetizes and stores energy, with the current flow as shown in diagram (a).

When Q1 turns off and the fast leg upper switch Q2 operates as a 1-D switch, the inductor demagnetizes, releasing its stored energy to the load, with the current flow as shown in diagram (b).

During the negative half-cycle of the input voltage, the slow leg SR2 conducts. When the fast leg upper switch Q2 operates as a D switch, the inductor magnetizes and stores energy, with the current flow as shown in diagram (c).

When Q2 turns off and the fast leg lower switch Q1 operates as a 1-D switch, the inductor demagnetizes, delivering its energy to the load, with the current flow as shown in diagram (d).



(a) During the positive half cycle: Q1 conducts as a D switch

(b) During the positive half cycle: Q2 conducts as a 1-D switch

(c) During the negative half cycle: Q2 conducts as a D switch

(d) During the negative half cycle: Q1 conducts as a 1-D switch

Figure 3 Operating Principle of Totem-pole PFC

OPERATING PRINCIPLE OF HP1010A

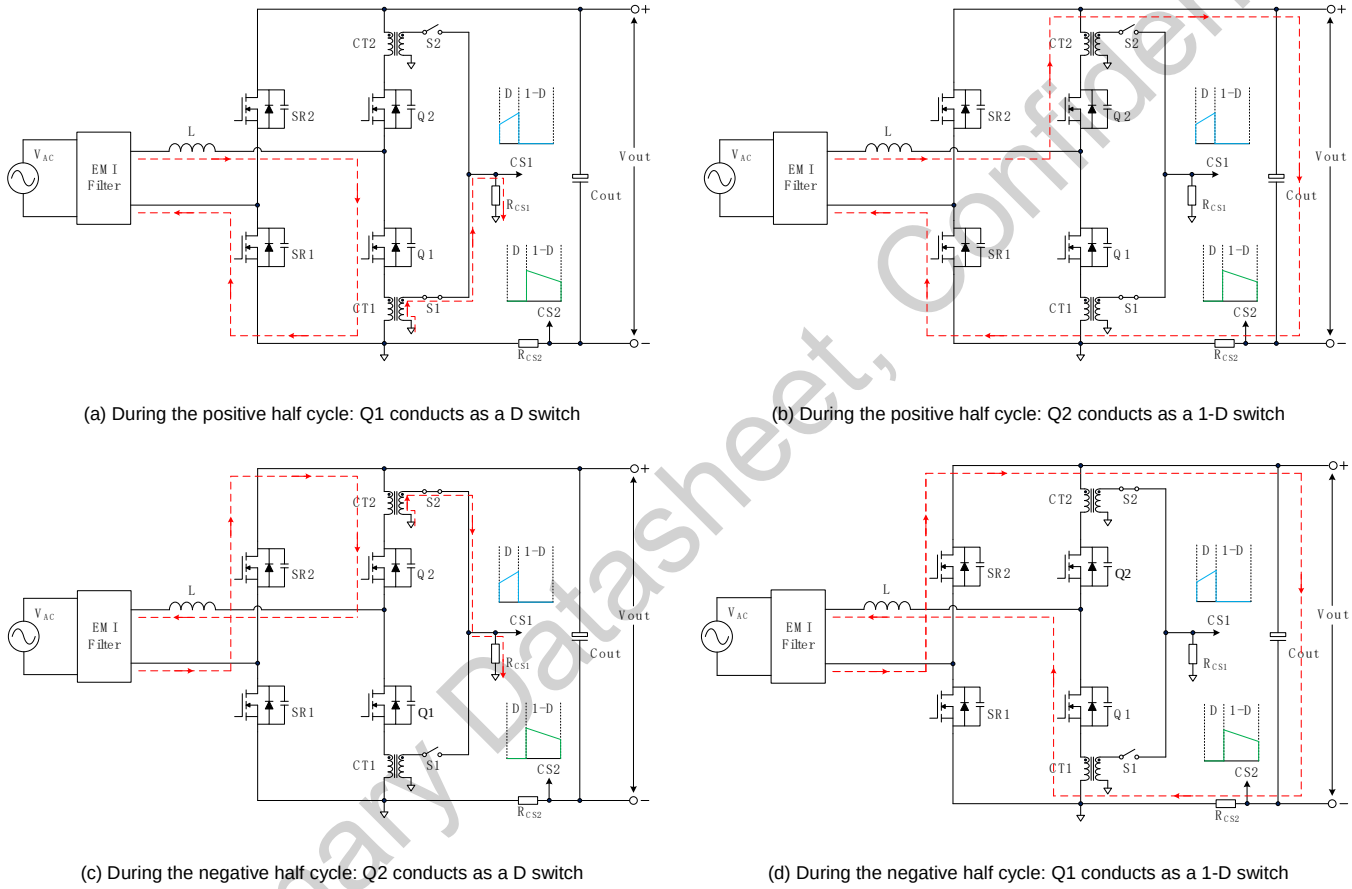
The operating principle of the Totem-pole PFC controller HP1010A is illustrated in Figure 4.

During the positive half-cycle of the input voltage: The slow leg SR1 conducts. When the fast leg lower switch Q1 operates as D switch, CS1 samples the magnetizing current. The inductor current path and magnetizing current sampling principle are shown in diagram (a). When the fast leg upper switch Q2 operates as a 1-D switch, CS2

samples the demagnetizing current. The inductor current path and demagnetizing current sampling principle are shown in diagram (b).

During the negative half-cycle of the input voltage: The slow leg SR2 conducts. When the fast leg upper switch Q2 operates as a D switch, CS1 samples the magnetizing current. The inductor current path and magnetizing current sampling principle are shown in diagram (c). When the fast leg lower switch Q1 operates as a 1-D switch, CS2 samples the demagnetizing current. The inductor current path and demagnetizing current sampling principle are shown in diagram (d).

By sampling the magnetizing current and demagnetizing current within a single switching cycle via CS1and CS2, respectively, the average current in a switching cycle obtained.



(a) During the positive half cycle: Q1 conducts as a D switch

(b) During the positive half cycle: Q2 conducts as a 1-D switch

(c) During the negative half cycle: Q2 conducts as a D switch

(d) During the negative half cycle: Q1 conducts as a 1-D switch

Figure 4 Operating Principle of The Totem-pole PFC Controller HP1010A

OPERATING MODES

The HP1010A operates in three modes depending on the load: CCM mode, DCM mode, and burst mode, as shown in Figure 5.

Under heavy load, the system operates in CCM, where the switching frequency is high and the PFC remains in continuous conduction mode.

Under light load, the system operates in DCM with a switching frequency of 30 kHz. the frequency is reduced to improve light-load efficiency.

Under no load, the system operates in burst mode.

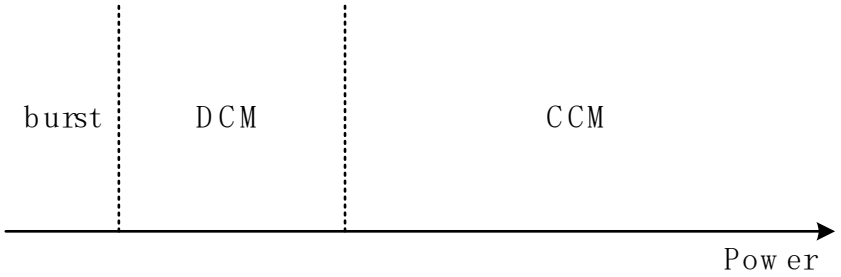


Figure 5 Operating Mode of HP1010A

In burst mode, the system operation is as shown in Figure 6. When the load falls below the system-set burst threshold, the PFC enters burst mode. In this mode, the PWM turns on when the input voltage lower than the output voltage reference. When the increase in the output voltage exceeds the set delta amount, the PWM turns off.

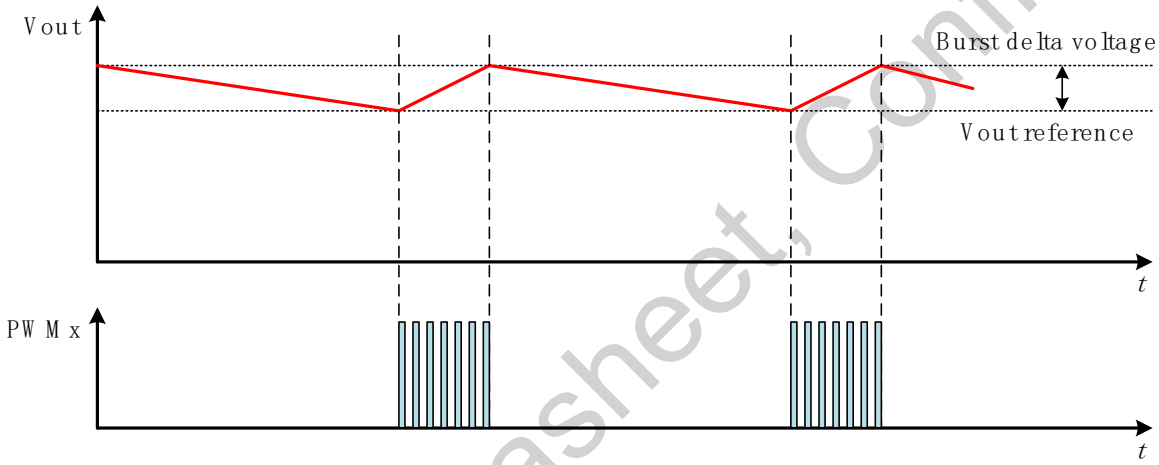


Figure 6 Burst Mode

AC LINE ZERO-CROSSING CONTROL STRATEGY

The unique zero-crossing control strategy of the HP1010A reduces switching stress when the slow leg turns on, resulting in a smoother discharge curve and lower discharge current.

Taking the transition from negative to positive of input voltage as an example, the control strategy is illustrated in Figure 7. When the input voltage approaches 0V from the negative side, the system detects that the PFC has entered the zero-crossing region, and all PWM pulses are turned off. When the system detects that the input voltage changes from negative to positive, after a certain debounce time, the PFC exits the zero-crossing region.

At this point, the voltage across the slow leg SR1, V_{DS}, is close to the output voltage. If SR1 were to turn on directly, it would experience high switching stress. Therefore, before SR1 turns on, the fast leg PWML is used to discharge the V_{DS} voltage across SR1.

HP1010A employs a two-stage open-loop pulse strategy, allowing independent configuration of the number of pulses in each stage and the pulse step size increment. In the first stage, a small step size is used to gradually discharge the V_{DS} voltage of SR1, minimizing discharge current. In the second stage, as V_{DS} voltage decreases, a larger step size is applied to further reduce V_{DS} voltage, achieving better discharge efficiency.

Once the open-loop pulse sequence completes, SR1 turns on with minimal switching stress.

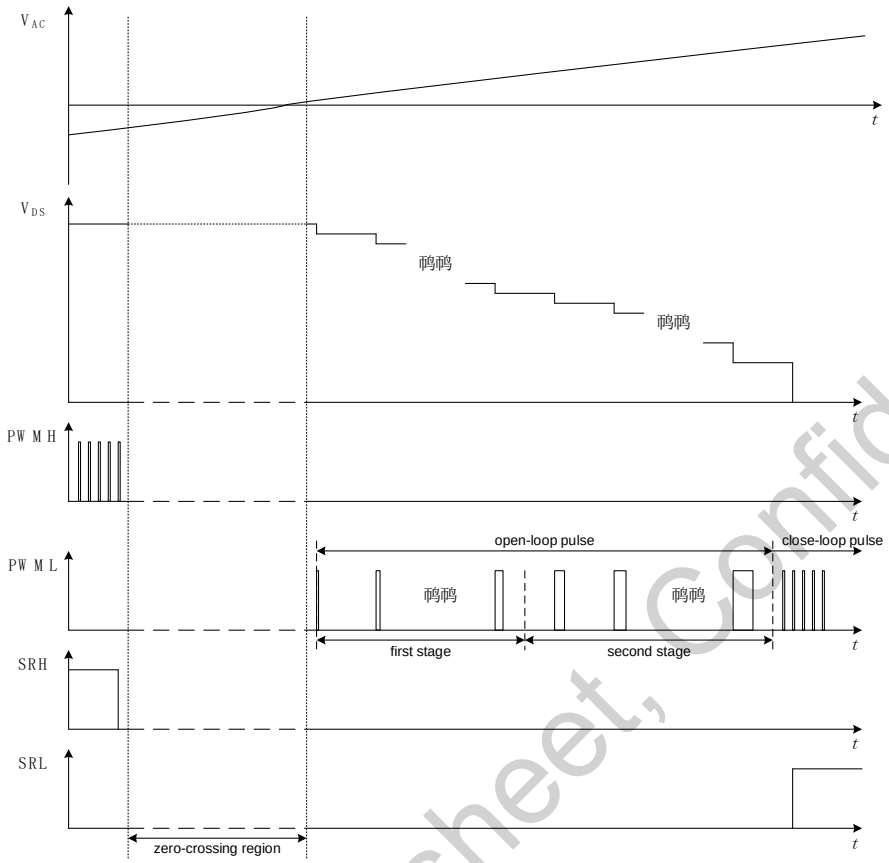


Figure 7 AC Line Zero-crossing Control Strategy

1-D SWITCH CONTROL

The turn-on and turn-off of the 1-D switch in HP1010A are controlled by two comparators respectively, namely CS2_OCP and CS2_ZCD.

CS2_OCP controls the turn-on of the 1-D switch: The reference value of the comparator is provided by a DAC, and the output reference voltage range of the DAC is 50 mV - 237 mV. The 1-D switch turns on when the demagnetization current signal sampled by the CS2 pin is greater than this reference value, and after a certain blanking time and debounce time.

CS2_ZCD controls the turn-off of the 1-D switch: The reference value of this comparator is also provided by a DAC, and the output reference voltage range of the DAC is 7.6 mV - 68 mV. The 1-D switch turns off when the demagnetization current signal sampled by the CS2 pin is less than this reference value, and after a certain blanking time and debounce time.

SYSTEM FUNCTIONS

SKIP MODE

To reduce the system's standby power consumption under no-load conditions, the SKIP function of HP1010A can control the power supply of the external driver chip or the enable of the driver chip through the SKIP signal when the PWM needs to be turned off in burst mode. The specific working mode is shown in Figure 8. When the PWM drive needs to be turned on, the SKIP signal will be set high in advance, and this advance amount can be configured via a register. When the PWM signal is turned off, the SKIP signal is pulled low with a delay to ensure that the PWM can be turned off reliably. This can reduce the standby power consumption of the driver chip.

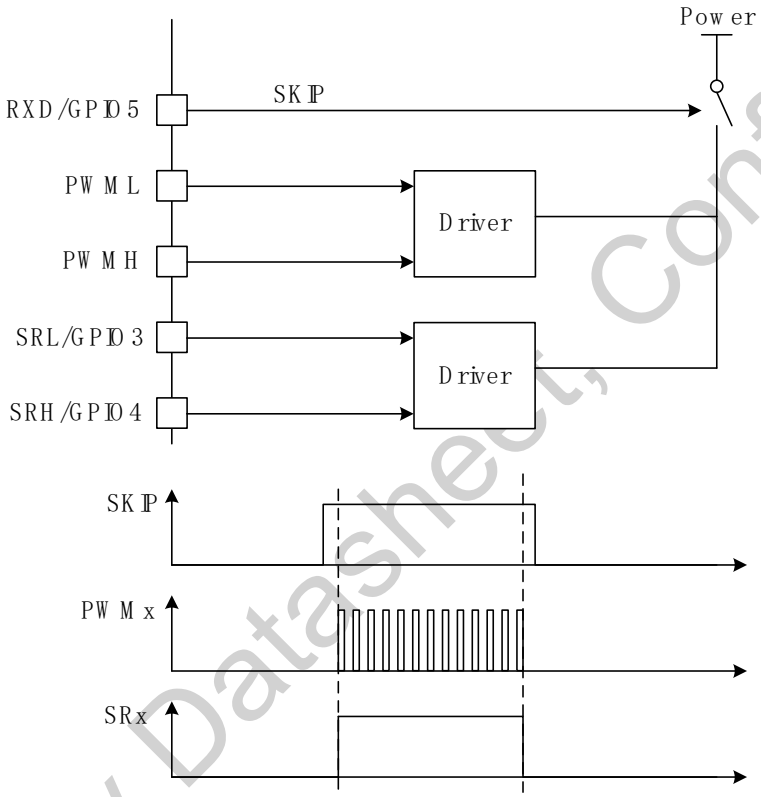


Figure 8 SKIP Mode

BUS VOLTAGE ADAPTIVE ADJUSTMENT BASED ON POWER

The output voltage of PFC can be adaptively adjusted according to the power, and its working principle is shown in Figure 9. When the system is in light-load burst mode, the output voltage can be configured to rise through a register, and the reference value of the output voltage at this time is V_{REF_SET} + V_{REF_BURST}. When the PFC exits the burst mode, the output voltage can be linearly adjusted according to the power. By setting the power points P_A and P_B, the reference voltage variation V_{REF_DELTA}, and the slope V_{REF_SLOPE} of the reference voltage changing with power determined thereby, the function of adaptive adjustment of the output voltage according to power can be realized. When the system exits the burst mode and the power is less than P_A, the output voltage reference value is V_{REF_SET}. When the power is greater than P_B, the bus voltage reference value is V_{REF_SET} + V_{REF_DELTA}. When the power is greater than P_A and less than P_B, the output voltage reference value changes between V_{REF_SET} and V_{REF_SET} + V_{REF_DELTA} at the slope V_{REF_SLOPE}.

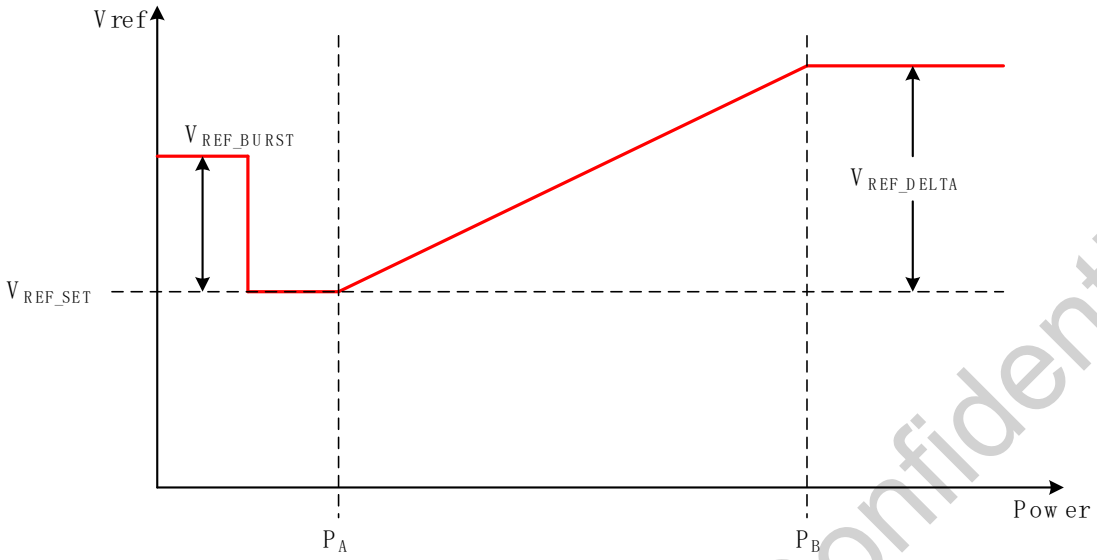


Figure 9 Bus Voltage Adaptive Adjustment Based on Power

RELAY POWER-SAVING FUNCTION

When the PFC operates under light load, the Relay can be turned off to reduce its driving loss for further improving the system efficiency. This function can be enabled and configured via registers. By setting the power threshold for turning off the Relay, the power point at which the Relay is turned off can be adjusted.

RELAY DELAY COMPENSATION FUNCTION

Since the Relay requires a certain amount of time to pull-in, if the Relay's control signal is issued at the zero-crossing point of the input voltage, the actual pull-in point of the Relay may end up at the peak of the input voltage due to the influence of the pull-in time, which will result in a relatively large inrush current. To solve this problem, HP1010A provides a Relay delay compensation function, as shown in Figure 10. After the pull-in delay of the relay is known, the Relay's delay compensation can be set through a register, so that the Relay's control signal is issued in advance of the zero-crossing point. This advance amount is the Relay's delay compensation value set by the register. In this way, the actual pull-in position of the Relay can be controlled near the zero-crossing point, reducing the inrush current during pull-in.

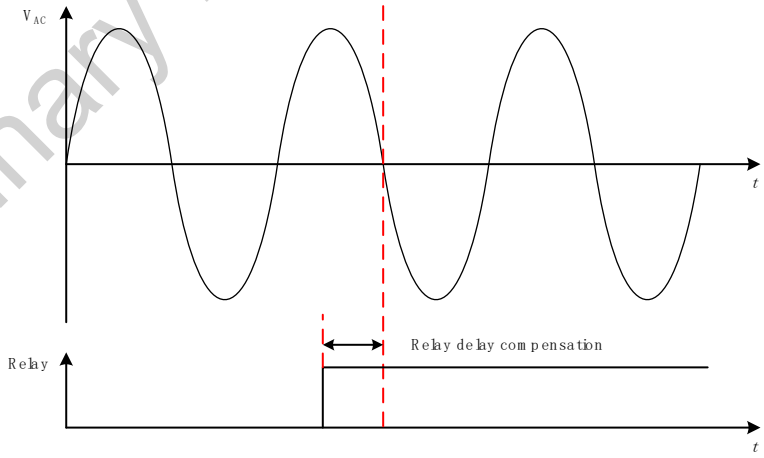


Figure 10 Relay Delay Compensation Function

PFC OK INDICATION

HP1010A can provide the working status of the front-stage PFC to the post-stage DCDC converter through the PFC OK pin, which is used to control the operation of the post - stage DCDC converter. During the start-up phase, after the

PFC detects that the system is normal, the output voltage reaches the set value after start-up, and a certain filtering time has elapsed, the PFC OK signal will be set high. After the PFC OK signal is set high, if the output voltage is detected to be lower than the set value or a fault occurs, the PFC OK signal will be set low.

X CAP COMPENSATION FUNCTION

HP1010A provides an X capacitor compensation function to improve the power factor of the PFC, and the compensation coefficient can be configured through a register. This function can be configured as enabled or disabled via a register.

METERING FUNCTION AND SYSTEM MONITORING

HP1010A can accurately calculate the effective values of input voltage and input current, thus enabling the reporting of input voltage, input current, and input power. Users can read relevant information such as input voltage, input current, input power, and output voltage from the chip through the communication interface. At the same time, they can also obtain the status information of system operation to monitor the system.

INPUT HIGH LINE AND LOW LINE DETECTION

HP1010A calculates the effective value of the input voltage, thus enabling it to obtain accurate input voltage information. The thresholds for high line and low line can be configured separately through registers. In this way, the system can set some system parameters respectively based on high line and low line detection, making the PFC configuration more flexible.

FREQUENCY DITHERING FUNCTION

HP1010A is equipped with a frequency dithering function, which can be used to optimize the system's EMI. Users can enable this function via a register, and configure the dithering width and dithering speed through registers as well. There are 4 selectable gears for the dithering width, which are ±12.5%, ±10.9%, ±7.8%, and ±6.25% respectively. For the speed of switching cycle variation, there are 8 selectable gears, namely 975.6 ns/ms, 487.8 ns/ms, 325.2 ns/ms, 243.8 ns/ms, 195.1 ns/ms, 162.6 ns/ms, 139.3 ns/ms, and 121.9 ns/ms.

PWM FREQUENCY SETTING

HP1010A has 8 basic configuration options for switching frequency, which are 20 kHz, 30 kHz, 45 kHz, 65.1 kHz, 89.9 kHz, 120.2 kHz, 160.2 kHz, and 198.4 kHz respectively. To meet customers' needs for different switching frequencies, fine-tuning can also be performed based on these 8 basic frequency gears. Through register configuration, an upward adjustment of 12.5%, 9.375%, 6.25%, 3.125% or a downward adjustment of 12.5%, 9.375%, 6.25%, 3.125% can be made on the basis of the above-mentioned frequencies.

FAULT AND PROTECTION

INPUT OVER-VOLTAGE PROTECTION

HP1010A features input voltage OVP protection. By calculating the effective value of the input voltage, it accurately implements input voltage OVP protection. The threshold for input voltage OVP protection can be configured via a register. The response to input overvoltage protection can also be configured through registers, with options including Ignore, Auto Recovery, and Latch.

INPUT FREQUENCY PROTECTION

HP1010A includes frequency protection. By monitoring the input voltage frequency, it triggers frequency protection and shuts down if the frequency falls outside the normal operating range of 40 Hz to 70 Hz.

OUTPUT OVER-VOLTAGE PROTECTION (OVP)

HP1010A provides two types of output over-voltage protection: Fast Output OVP and Slow Output OVP.

Fast Output OVP: Implemented via a hardware comparator. The over-voltage protection reference can be set using the DAC. Fast OVP is triggered when the sampled feedback of the output voltage exceeds this reference value. The response to fast output OVP can be configured via registers, with options including Ignore (PWM pulse shutdown), Auto Recovery, and Latch.

Slow Output OVP: Samples the output voltage via the ADC and performs over-voltage detection using internal digital logic. The over-voltage protection threshold can be set via a register. The response to slow output OVP can be configured via registers, with options including Ignore (PWM pulse shutdown), Auto Recovery, and Latch.

OUTPUT VOLTAGE SENSING SHORT-CIRCUIT PROTECTION

HP1010A detects an output voltage sensing short-circuit by monitoring the output voltage. If the output voltage remains below a system-set value for a period of time, a sensing short-circuit is determined. The response to this protection can be configured via registers, with options including Ignore, Auto Recovery, and Latch.

CYCLE-BY-CYCLE (CBC) OVER-CURRENT PROTECTION

HP1010A features Cycle-by-Cycle (CBC) over-current protection. The CBC over-current protection points for both high and low voltages can be configured separately via registers. The response to CBC protection can be configured via registers, with options including Ignore (PWM pulse shutdown), Auto Recovery, and Latch.

AVERAGE CURRENT OVER-CURRENT PROTECTION

HP1010A includes average current over-current protection, which can be enabled via register configuration. The current threshold for average current over-current protection can be set via a register. The response to this protection can be configured via registers, with options including Ignore, Auto Recovery, and Latch.

OVER-POWER PROTECTION

Leveraging its power metering functionality, the HP1010A provides overpower protection. The overpower protection threshold can be set via a register. The response to overpower protection can be configured via registers, with options including Ignore, Auto Recovery, and Latch.

NTC OVER-TEMPERATURE PROTECTION

When the NTC/ROV pin of the HP1010A is used as an external over-temperature protection detection pin, it sources a current of 46 µA. When an external thermistor is connected and the voltage at the NTC/ROV pin drops below 0.4 V, over-temperature protection is triggered. The protection resets when the voltage at the NTC/ROV pin rises above 0.8 V. The response to over-temperature protection can be configured via registers, with options including Ignore, Auto Recovery, and Latch.

ROV REDUNDANT OUTPUT OVER-VOLTAGE PROTECTION

In applications requiring high reliability, a second independent output overvoltage protection is necessary. HP1010A provides a second redundant output overvoltage protection path through the NTC/ROV pin. The overvoltage

protection threshold can be set using the internal DAC. When the output voltage feedback exceeds this protection point, an internal comparator is triggered, initiating the redundant output overvoltage protection. The response to redundant OVP can be configured via registers, with options including Ignore, Auto Recovery, and Latch.

COMMUNICATION AND EEPROM

HP1010A supports I²C communication and UART communication, and is equipped with a built-in 128-byte EEPROM. Users can modify the chip configuration via either I²C communication or UART communication, program the modified configuration into the EEPROM, and also monitor the system status.

I²C COMMUNICATION

I²C communication consists of only two wires, namely the Serial Clock Line (SCL) and the Serial Data Line (SDA). The data to be transmitted is sent through the SDA line and synchronized with the clock signal from SCL. As shown in Figure 11, all devices on the I²C network are connected to the same SCL and SDA lines. The default I²C address of the chip is 0x47.

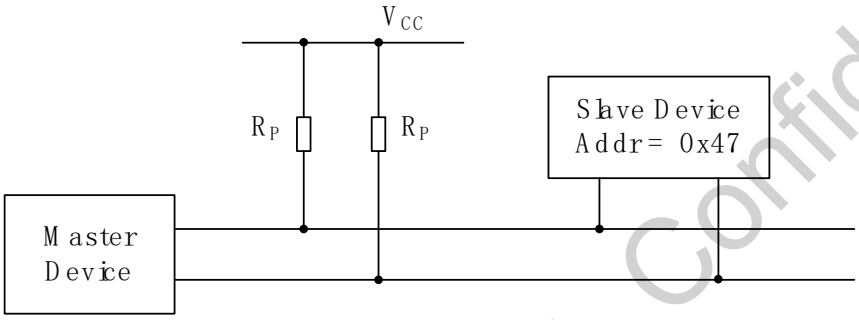


Figure 11 I²C Communication

UART COMMUNICATION

In addition to I²C communication, HP1010A also communicates with external devices using the standard UART protocol via two dedicated pins. The UART serial interface allows users to modify registers and read system status. When enabling UART communication, it is necessary to configure the pins RXD/GPIO5 and TXD/GPIO6 as the RXD pin and TXD pin for UART communication.

EEPROM

HP1010A is equipped with a built-in 128 bytes EEPROM, which is used to store user configurations. When the digital core and EEPROM are powered on, the chip loads these configurations from the EEPROM. When the chip loads the EEPROM configuration, it performs a CRC check to ensure the reliability of configuration loading. Users can program the configuration into the EEPROM via I²C.

APPLICATION INFORMATION

TOTEM POLE POWER FACTOR CORRECTION

Typical totem-pole PFC (TPPFC) application circuit is shown in Figure 12.

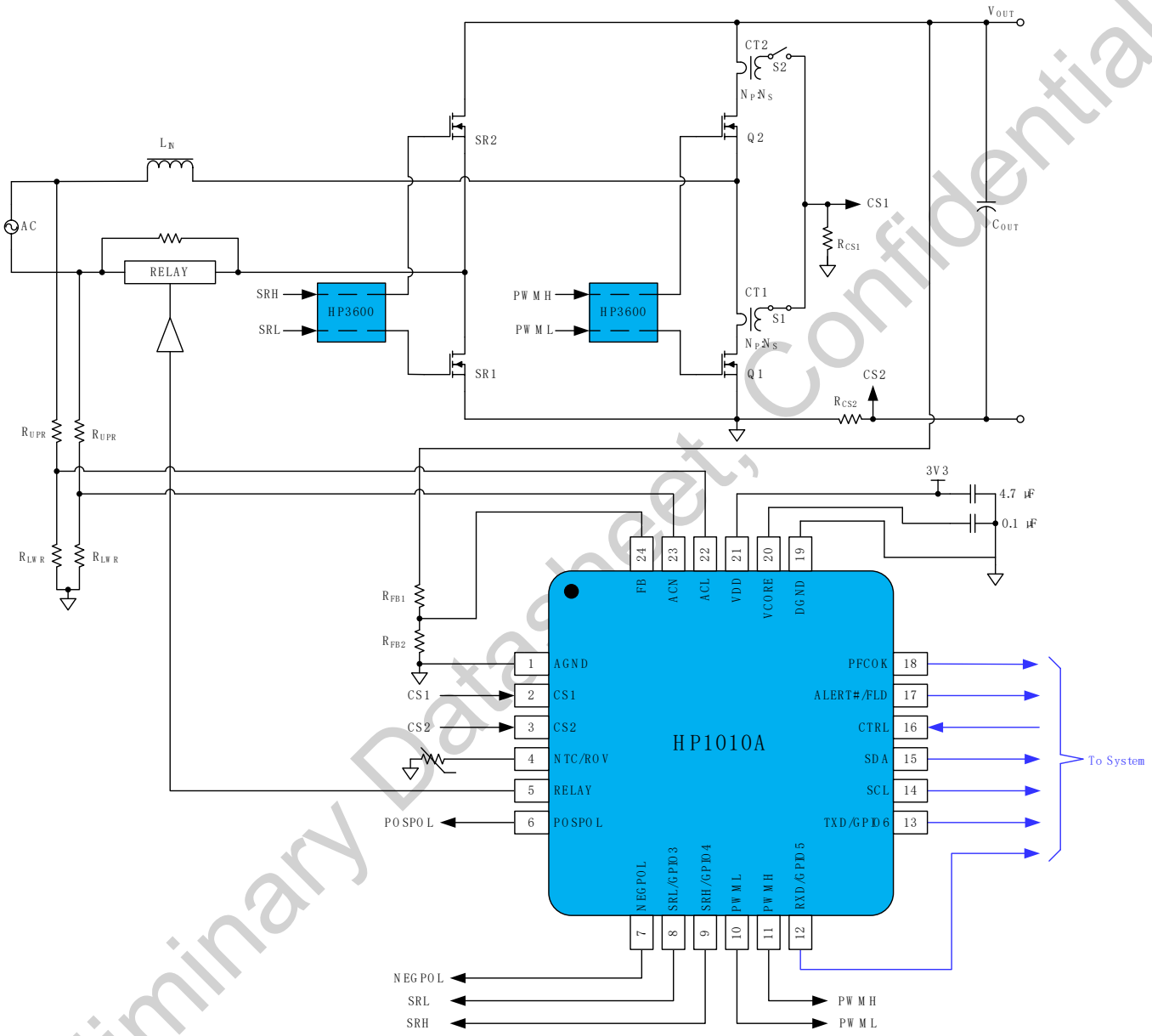
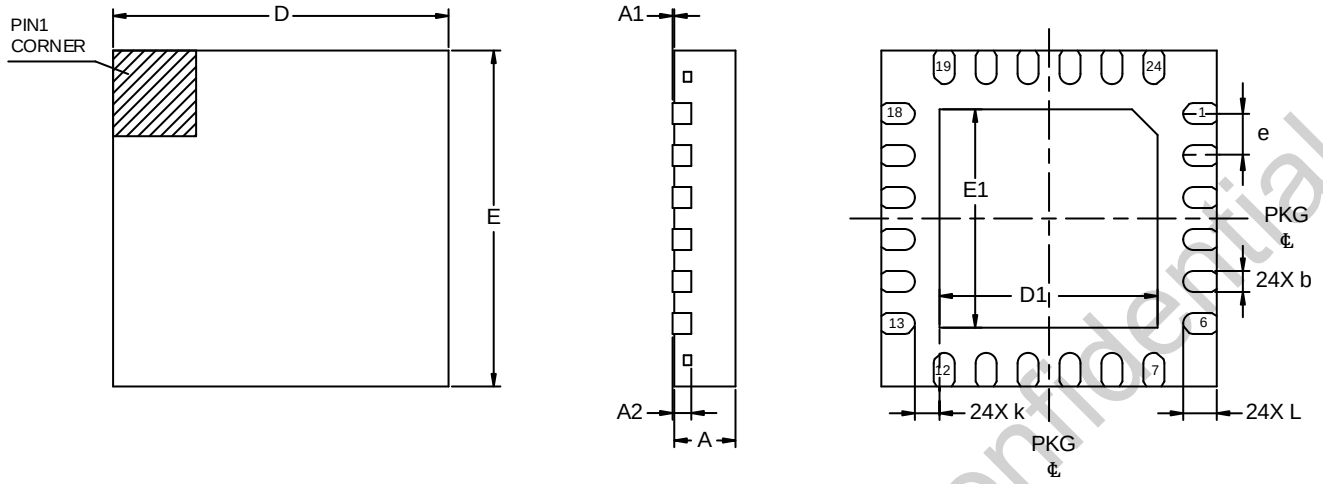


Figure 12 Totem Pole PFC Typical Application Circuit

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D1	2.40	2.70	2.80
E1	2.40	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN	

Figure 13 HP1010A-AA000-QN24R Dimension

PACKAGE TOP MARKING

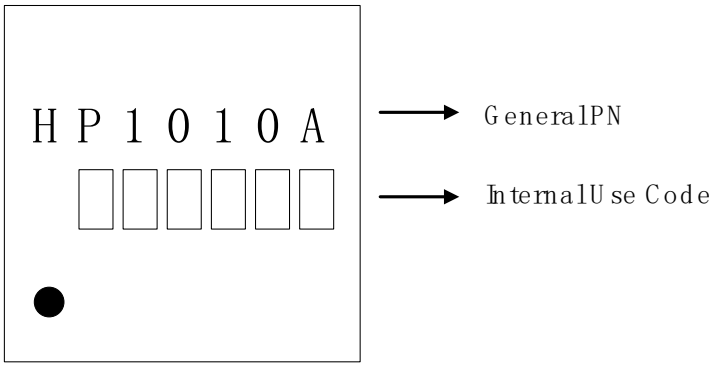


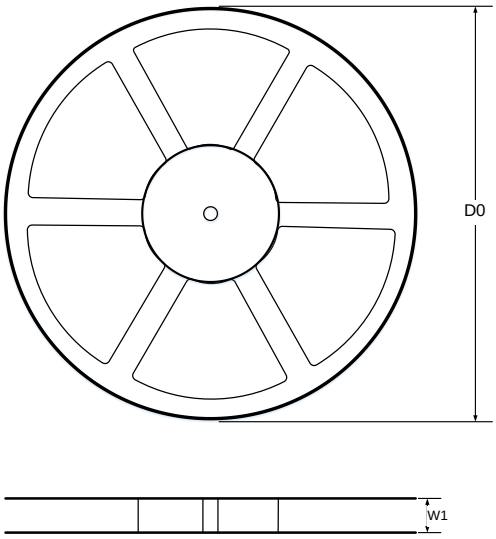
Figure 14 HP1010A-AA000-QN24R Package Top Marking

ORDERING GUIDE

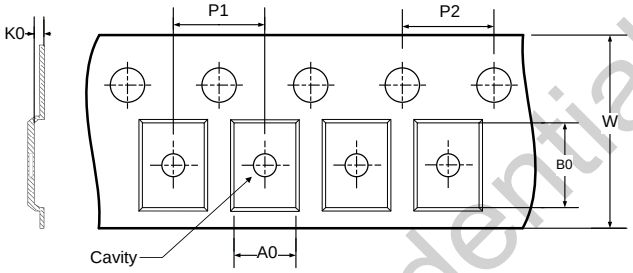
Model	Temperature Range	Package Type	MSL	Package Option	Quantity
HP1010A-AA000-QN24R	-40°C to +125°C	QFN4x4-24L	3	T&R	5000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

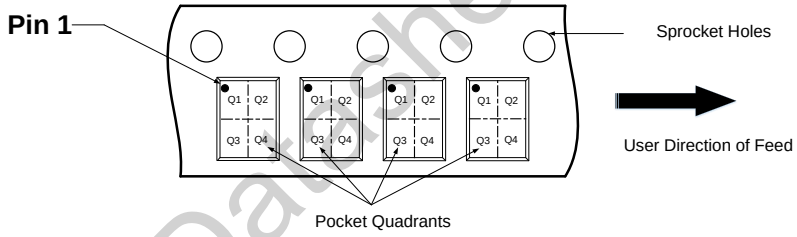


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP1010A-AAXXX-QN24R	QFN4X4-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Figure 15 Tape and Reel Information

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