General Description

The GreenMOS® SuperSi series is based on Oriental Semiconductor's unique device design to achieve extremely fast switching characteristics. It is the perfect replacement for the SiC device in high frequency operations with better ruggedness and cost. It is targeted to meet the most aggressive efficiency standards of power supply systems by pushing both performance and power density to extreme limits.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low reverse recovery charges
- Extremely low switching loss
- Excellent stability and uniformity

Applications

- EV motor driving system
- PV converter

Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
$I_{D,\ pulse}$	240	A
$R_{DS(ON),\ typ}$ @ V_{GS}=10V	22	mΩ
Q_g	353	nC

Marking Information

Product Name	Package	Marking
OSS100N65H6MF	TO247-Plus	OSS100N65H6M

Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	±30	V
Continuous drain current[1], T_C=25 °C	I_D	100	A
Continuous drain current[1], T_C=100 °C		63	
Pulsed drain current[2], T_C=25 °C	$I_{D,\ pulse}$	240	A
Power dissipation[3], T_C=25 °C	P_D	510	W
Single pulsed avalanche energy[5]	E_{AS}	2109	mJ
MOSFET dv/dt ruggedness, V_{DS}=0…480 V	dv/dt	50	V/ns
Reverse diode dv/dt, V_{DS}=0…480 V, I_{SD}≤I_D	dv/dt	50	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	650			V	V_{GS}=0 V, I_D=2 mA
Gate threshold voltage	$V_{GS(th)}$	3.0		5.0	V	V_{DS}=V_{GS}, I_D=2 mA
Drain-source on-state resistance	$R_{DS(ON)}$		22	25	mΩ	V_{GS}=18 V, I_D=50 A
			55			V_{GS}=18 V, I_D=50 A, T_j=150 °C
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=30 V
				-100		V_{GS}=-30 V
Drain-source leakage current	I_{DSS}			10	μA	V_{DS}=650 V, V_{GS}=0 V
Gate resistance	R_G		1.3		Ω	f=1 MHz, Open drain

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		10200		pF	V_{GS}=0 V, V_{DS}=50 V, f=100 kHz
Output capacitance	C_{oss}		665		pF	
Reverse transfer capacitance	C_{rss}		16		pF	
Effective output capacitance, energy related	$C_{o(er)}$		407		pF	V_{GS}=0 V, V_{DS}=0 V-400 V
Effective output capacitance, time related	$C_{o(tr)}$		1800		pF	
Turn-on delay time	$t_{d(on)}$		20		ns	V_{GS}=18 V, V_{DS}=400 V, R_G=2 Ω, I_D=40 A
Rise time	t_r		31		ns	
Turn-off delay time	$t_{d(off)}$		107		ns	
Fall time	t_f		6		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		353		nC	V_{GS}=18 V, V_{DS}=400 V, I_D=40 A
Gate-source charge	Q_{gs}		107		nC	
Gate-drain charge	Q_{gd}		93		nC	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			2.5	V	I_S=100 A, V_{GS}=0 V
Reverse recovery time	t_{rr}		62		ns	V_R=400 V, I_S=40 A, di/dt=1000A/μs
Reverse recovery charge	Q_{rr}		1.21		μC	
Peak reverse recovery current	I_{rrm}		36.2		A	

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) V_{DD}=100 V, V_{GS}=10 V, L=75 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams

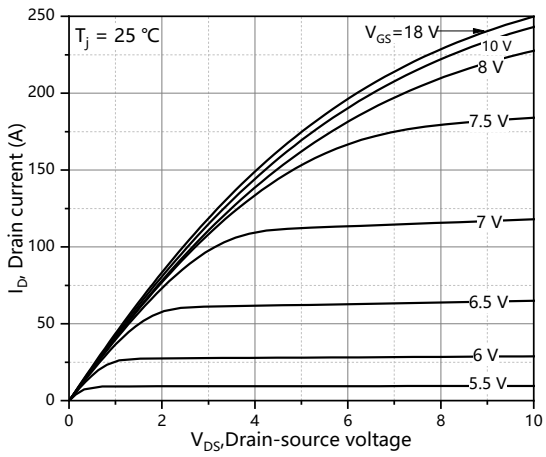

Figure 1. Typ. output characteristics

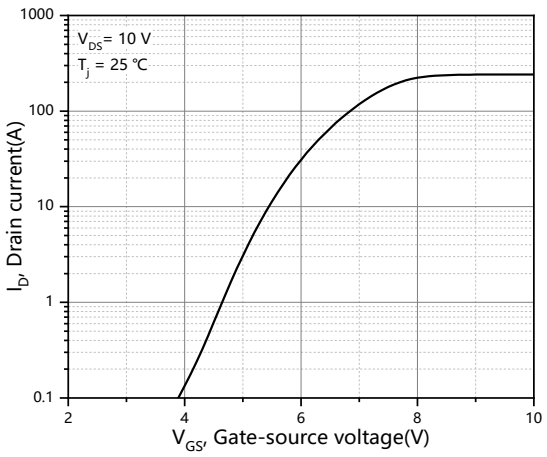

Figure 2. Typ. transfer characteristics

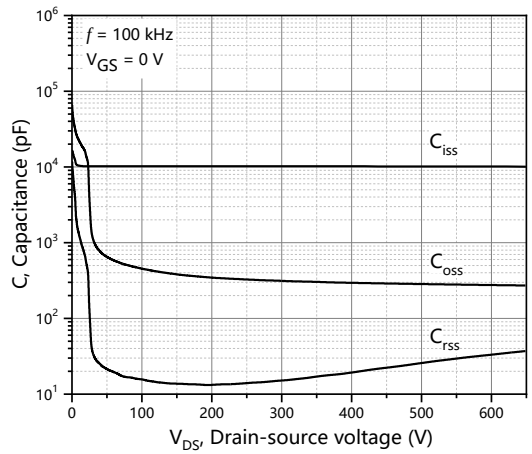

Figure 3. Typ. capacitances

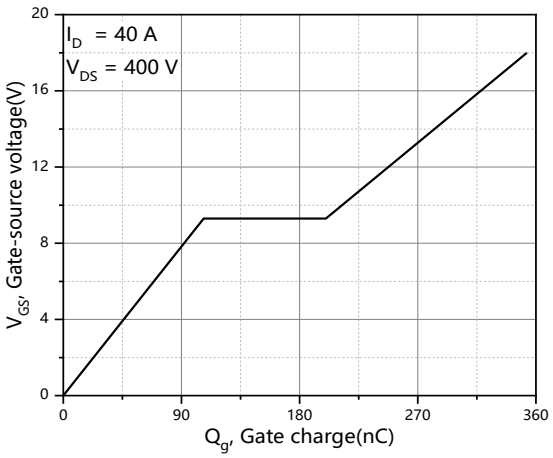

Figure 4. Typ. gate charge

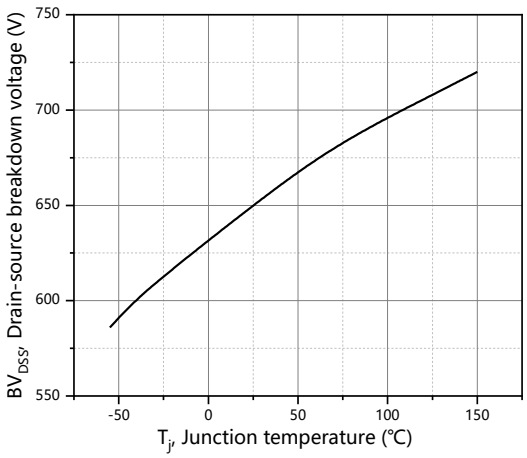

Figure 5. Drain-source breakdown voltage

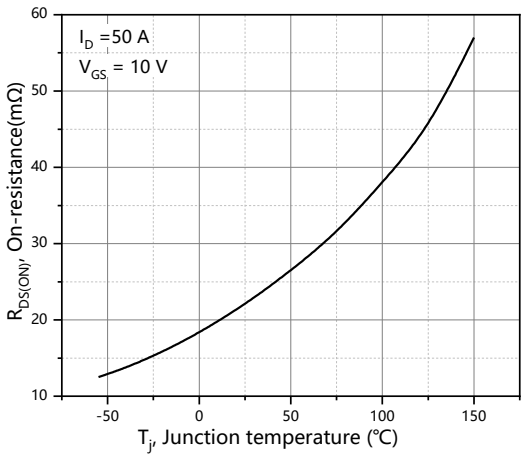

Figure 6. Drain-source on-state resistance

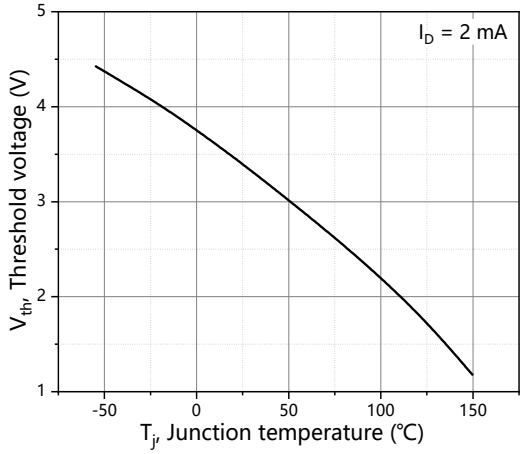

Figure 7. Threshold voltage

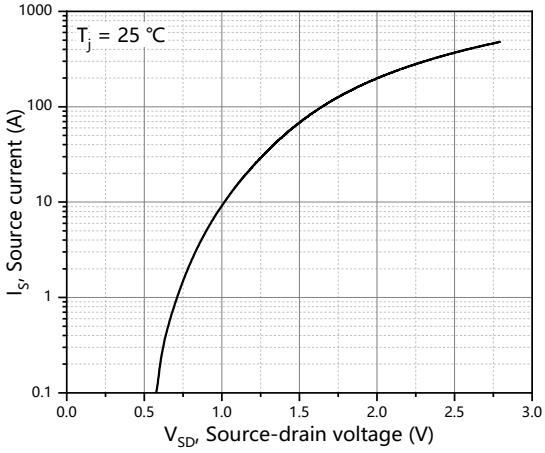

Figure 8. Forward characteristic of body diode

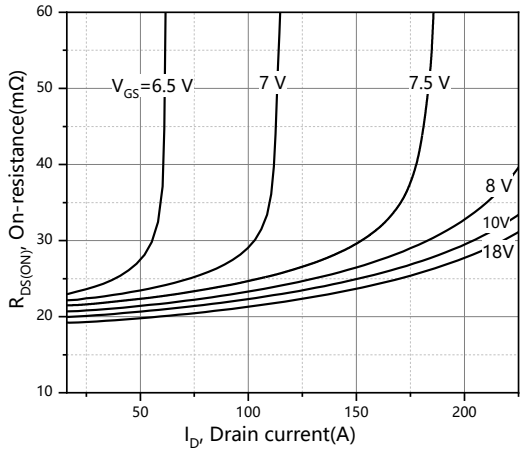

Figure 9. Drain-source on-state resistance

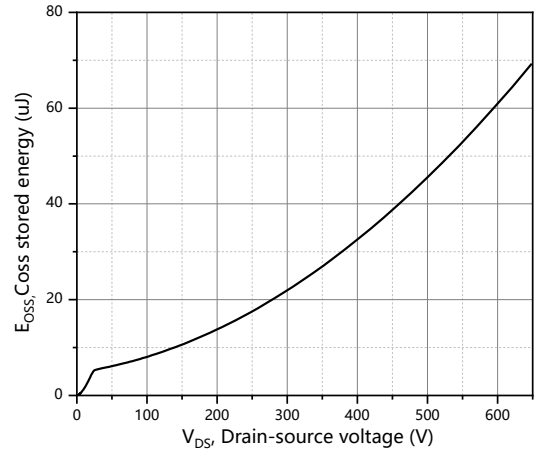

Figure 10. Typ. Coss stored energy

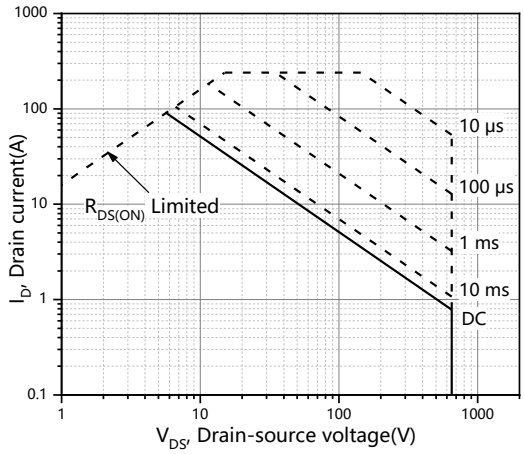

Figure 11. Safe operation area T_C=25 °C

Test circuits and waveforms

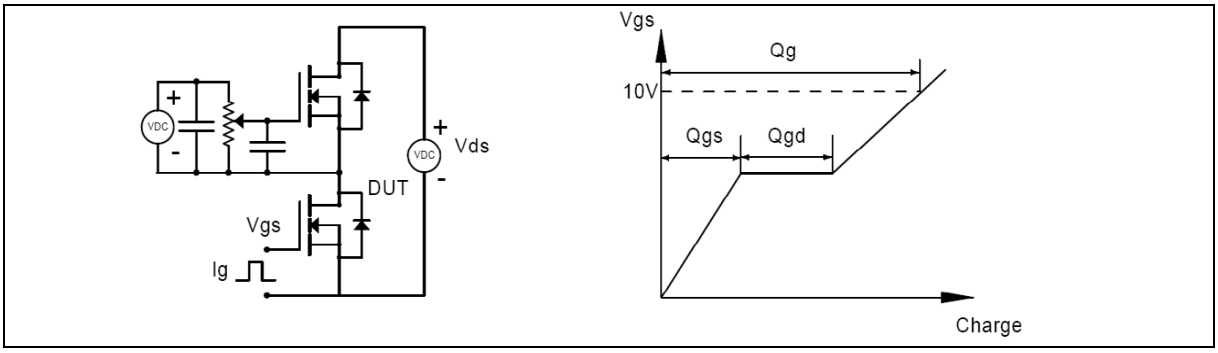

Figure 1. Gate charge test circuit & waveform

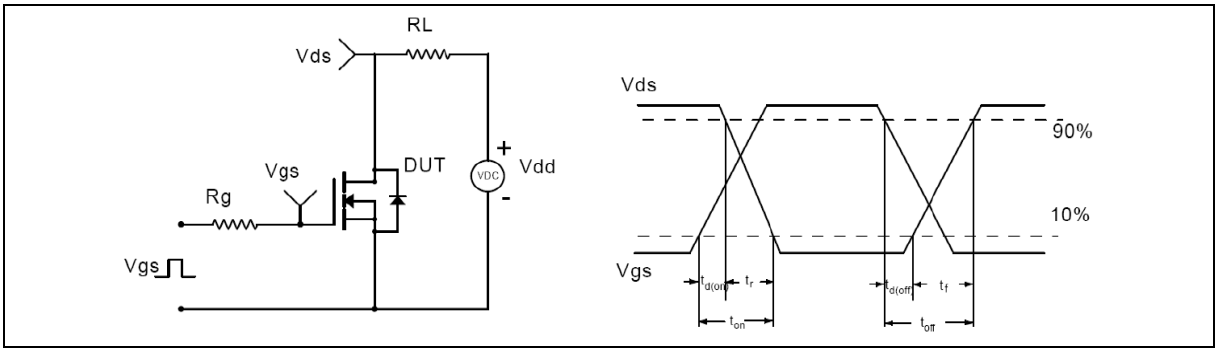

Figure 2. Switching time test circuit & waveforms

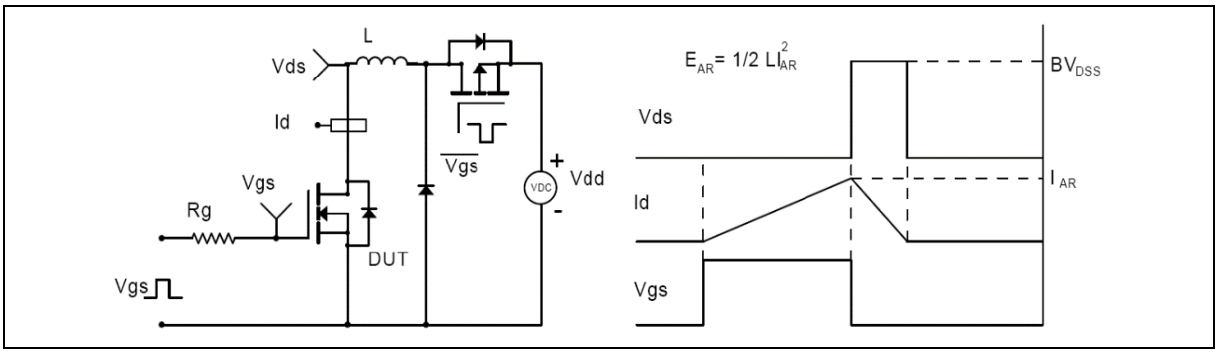

Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

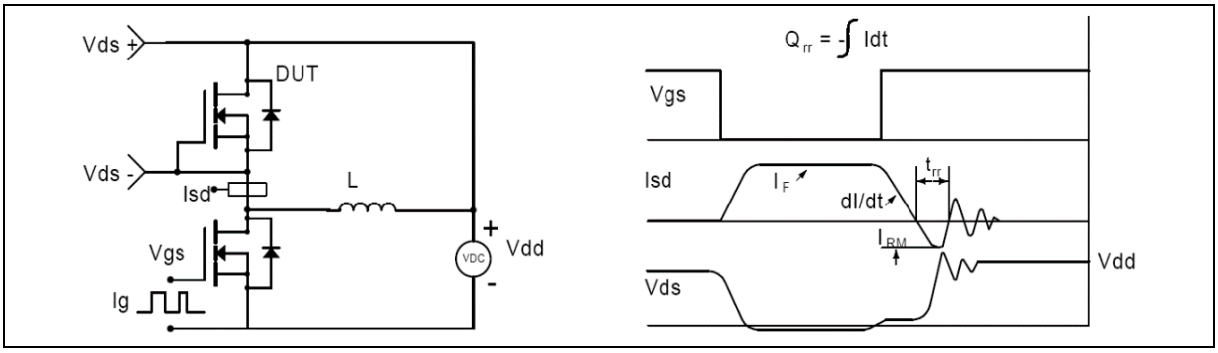

Figure 4. Diode reverse recovery test circuit & waveforms

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
OSS100N65H6MF	TO247-Plus	yes	yes	yes

Legal Disclaimer

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