

General Description

The GreenMOS[®] high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

The GreenMOS[®] Z series is integrated with fast recovery diode (FRD) to minimize reverse recovery time. It is suitable for resonant switching topologies to reach higher efficiency, higher reliability and smaller form factor.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity

GreenMOS[®]



Applications

- LED lighting
- Telecom
- Adapter
- Sever
- Solar/UPS

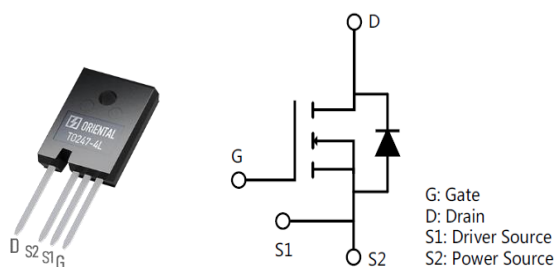
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
I_D , pulse	330	A
$R_{DS(ON)}$, max @ $V_{GS}=10V$	22	m Ω
Q_g	212	nC

Marking Information

Product Name	Package	Marking
OSG65R022H4T3ZF-F	TO247-4L	OSG65R022H4T3Z

Package & Pin Information



Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_D	110	A
Continuous drain current ¹⁾ , $T_C=100^{\circ}\text{C}$		70	
Pulsed drain current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{D, \text{pulse}}$	330	A
Continuous diode forward current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_S	110	A
Diode pulsed current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{S, \text{pulse}}$	330	A
Power dissipation ³⁾ , $T_C=25^{\circ}\text{C}$	P_D	652	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	2250	mJ
MOSFET dv/dt ruggedness, $V_{DS}=0\ldots 400\text{ V}$	dv/dt	100	V/ns
Reverse diode dv/dt, $V_{DS}=0\ldots 400\text{ V}$, $I_{SD}\leq I_D$	dv/dt	50	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^{\circ}\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.19	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	$^{\circ}\text{C/W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	650			V	$V_{GS}=0\text{ V}$, $I_D=2\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3		5	V	$V_{DS}=V_{GS}$, $I_D=2\text{ mA}$
Drain-source on-state resistance	$R_{DS(on)}$		18.5	22	m Ω	$V_{GS}=10\text{ V}$, $I_D=55\text{ A}$
			45.5			$V_{GS}=10\text{ V}$, $I_D=55\text{ A}$, $T_j=150^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=30\text{ V}$
				-100		$V_{GS}=-30\text{ V}$
Drain-source leakage current	I_{DSS}			10	μA	$V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$
Gate resistance	R_G		1.5		Ω	$f=1\text{ MHz}$, Open drain

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		9289		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		560		pF	
Reverse transfer capacitance	C_{rss}		5.3		pF	
Effective output capacitance, energy related	$C_{o(er)}$		343		pF	$V_{GS}=0\text{ V}$, $V_{DS}=0\text{ V}-400\text{ V}$
Effective output capacitance, time related	$C_{o(tr)}$		2150		pF	
Turn-on delay time	$t_{d(on)}$		40		ns	$V_{GS}=10\text{ V}$, $V_{DS}=400\text{ V}$, $R_G=2\ \Omega$, $I_D=40\text{ A}$
Rise time	t_r		43		ns	
Turn-off delay time	$t_{d(off)}$		108		ns	
Fall time	t_f		3		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		212		nC	$V_{GS}=10\text{ V}$, $V_{DS}=400\text{ V}$, $I_D=40\text{ A}$
Gate-source charge	Q_{gs}		59		nC	
Gate-drain charge	Q_{gd}		89		nC	
Gate plateau voltage	$V_{plateau}$		6.7		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	$I_S=110\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		209		ns	$V_R=400\text{ V}$, $I_S=40\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		2		μC	
Peak reverse recovery current	I_{rrm}		17.4		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $L=80\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

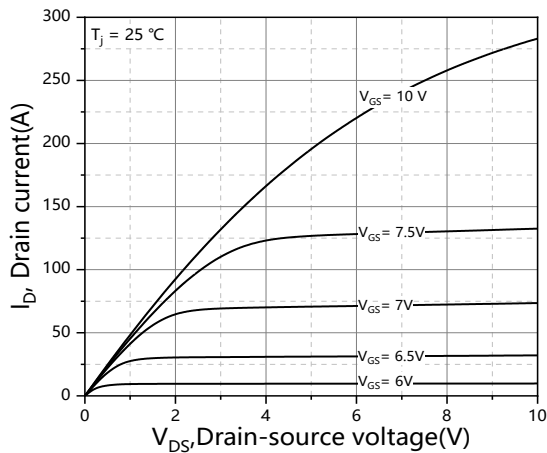


Figure 1. Typ. output characteristics $T_j=25^{\circ}\text{C}$

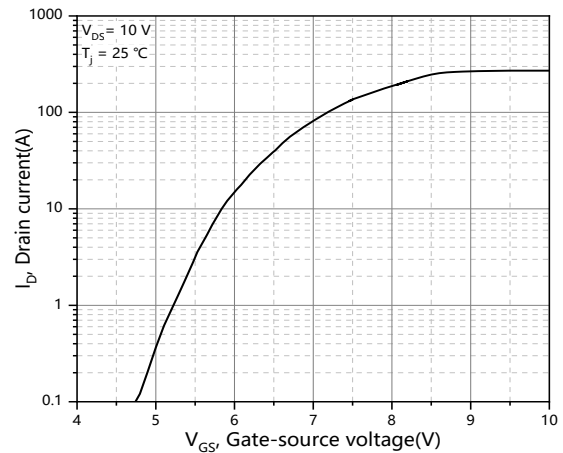


Figure 2. Typ. transfer characteristics

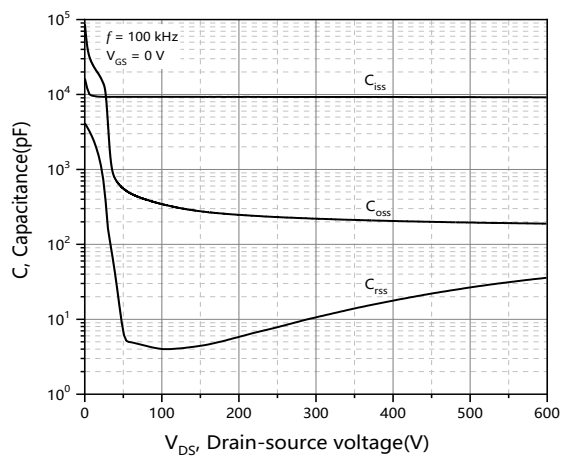


Figure 3. Typ. capacitances

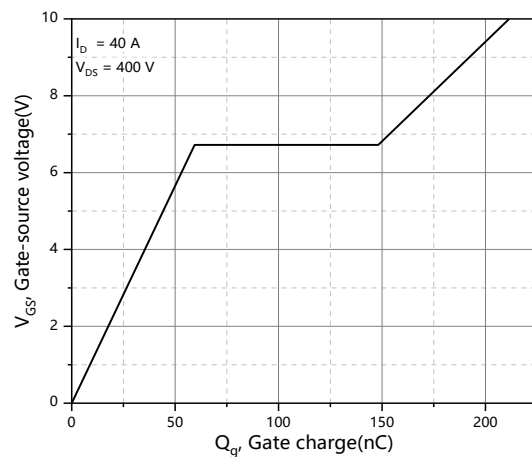


Figure 4. Typ. gate charge

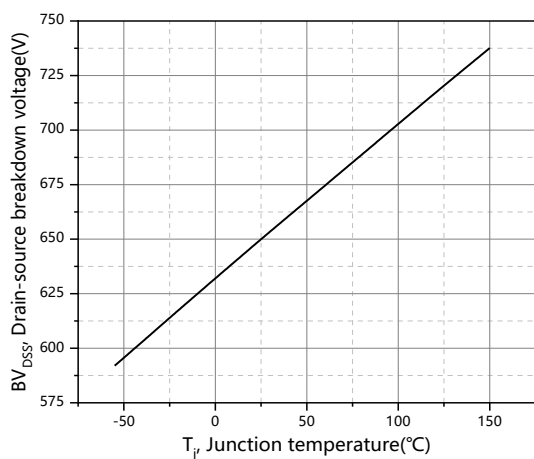


Figure 5. Drain-source breakdown voltage

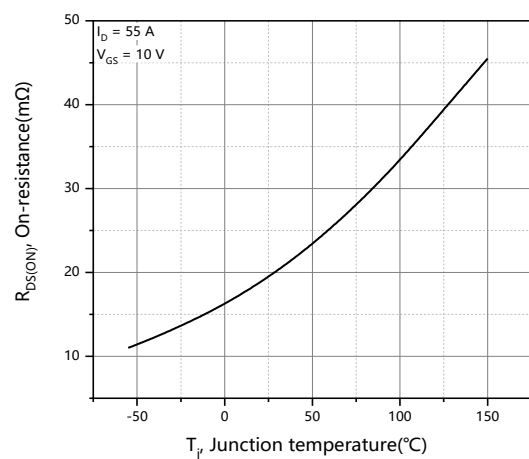


Figure 6. Drain-source on-state resistance

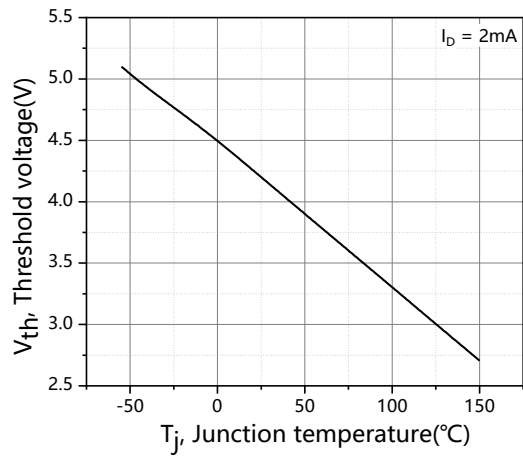


Figure 7. Threshold voltage

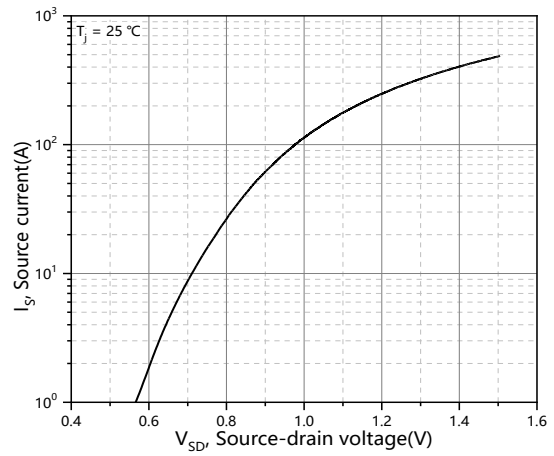


Figure 8. Forward characteristic of body diode

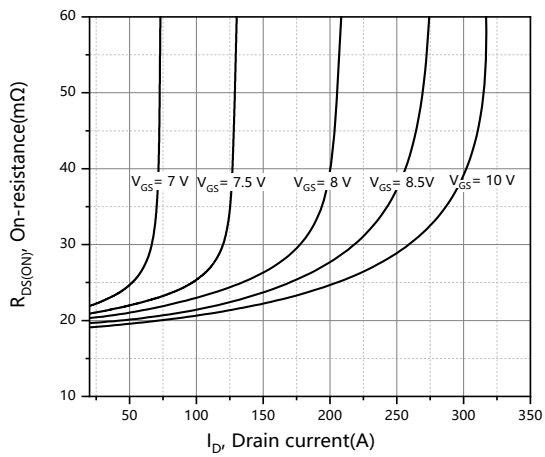


Figure 9. Drain-source on-state resistance

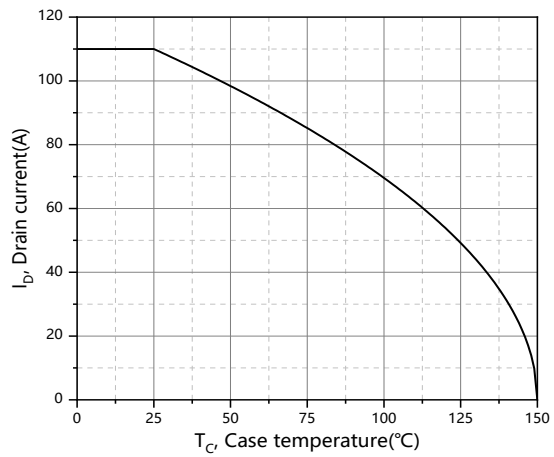


Figure 10. Drain current

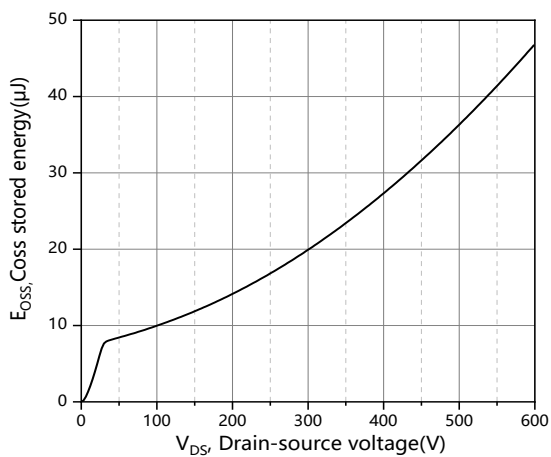


Figure 11. Typ. Coss stored energy

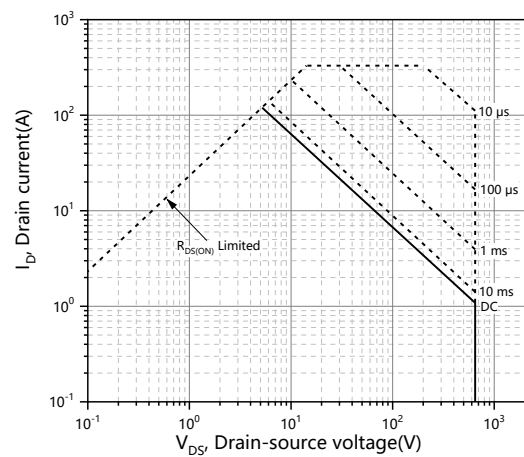


Figure 12. Safe operation area Tc=25°C

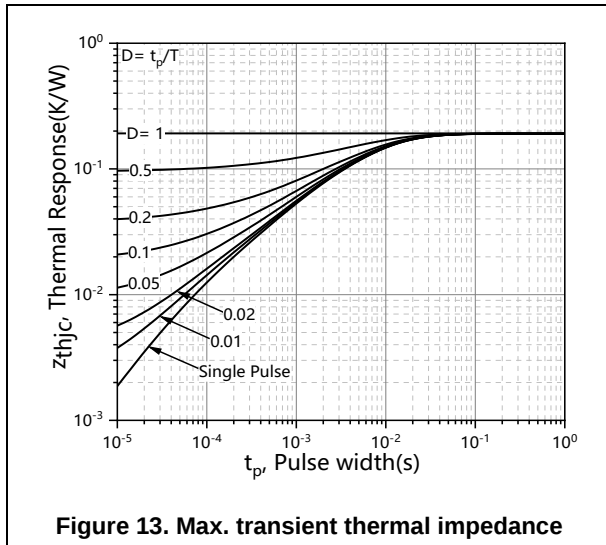


Figure 13. Max. transient thermal impedance

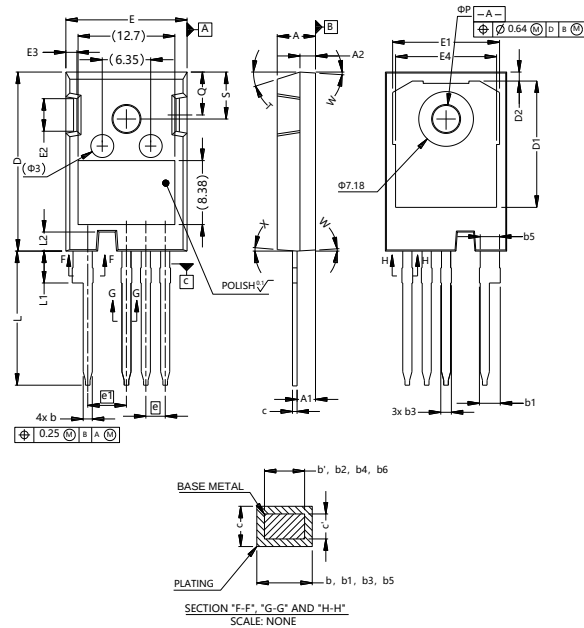
Figure 1 consists of two parts. The left part is a circuit diagram of the measurement setup. It shows a Differential Under Test (DUT) connected to a DC voltage source V_{ds} and a DC voltage source V_{gs} . A gate current I_g is applied to the gates of the DUT. The right part is a graph of V_{gs} versus Charge. The graph shows a characteristic with a plateau at $10V$. The total charge Q_g is indicated by a dashed line. The gate charge Q_{gs} and the gate-drain charge Q_{gd} are also indicated.

The circuit diagram on the left shows a MOSFET (DUT) with its gate connected to a voltage source V_{gs} through a resistor R_g . The drain is connected to a load inductor L and a load capacitor C_L in parallel. The gate is biased at V_{ds} and the drain is biased at V_{dd} . The drain current is I_d . The waveforms on the right show the gate voltage V_{gs} as a square wave, the drain current I_d as a triangular wave during the switching transient, and the drain voltage V_{ds} as a square wave. The energy stored in the inductor is given by $E_{AR} = 1/2 L I_{AR}^2$.

The figure consists of two parts. On the left is a schematic diagram of the switching device. It features a MOSFET with a DUT (Device Under Test) connected to its drain. The drain is also connected to an inductor L, which is then connected to a VDD source. The gate of the MOSFET is driven by a signal Vgs, and the source is connected to a signal Ig. The drain voltage is labeled Vds. On the right is a set of waveforms showing the switching behavior. The top waveform is Vgs, which transitions from low to high. The middle waveform is Isd (source-drain current), which rises to a value I_F during the forward conduction phase, then falls during the reverse recovery phase, characterized by a time t_rr. The bottom waveform is Vds (drain-source voltage), which is low during forward conduction and rises to VDD during reverse recovery. The formula $Q_{rr} = -\int I_d t$ is shown above the waveforms, indicating the calculation of reverse recovery charge.

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Package Information



Symbol	mm	
	Min	Max
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
c'	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
ΦP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF	
W	3.5° REF	
X	4° REF	

Version: TO247-4L-S package outline dimension

Ordering Information

Package Type	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO247-4L-S	30	15	450	4	1800

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
OSG65R022H4T3ZF-F	TO247	yes	yes	yes

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