Features

- Output Current of 150mA
- Thermal Overload Protection
- Short Circuit Protection
- Output transistor safe area protection
- No external components
- Package：SOT23, SOT89-3 and TO92

General Description

OSU78LXX is three-terminal positive regulators. One of these regulators can deliver up to 150 mA of output current. The internal limiting and thermal -shutdown features of the regulator make them essentially immune to overload. When used as a replacement for a zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower quiescent current.

Selection Table

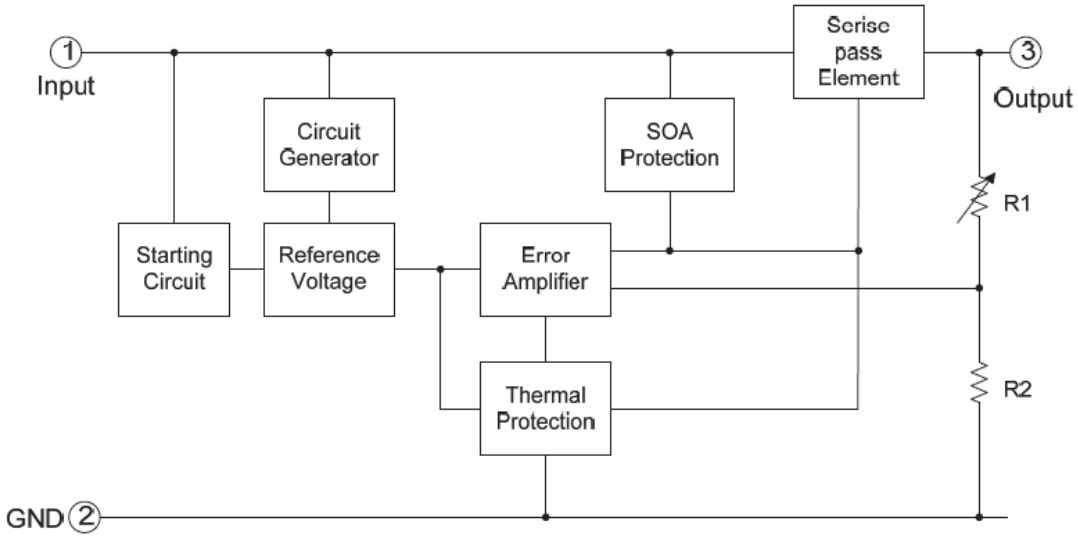
Part No.	Output Voltage	Package	Marking
OSU78L33-XX-AV	3.3V	SOT23 SOT89-3 TO92	78L33/XXxxx
OSU78L05-XX-AV	5.0V		78L05/XXxxx
OSU78L06-XX-AV	6.0V		78L06/XXxxx
OSU78L08-XX-AV	8.0V		78L08/XXxxx
OSU78L09-XX-AV	9.0V		78L09/XXxxx
OSU78L10-XX-AV	10.0V		78L10/XXxxx
OSU78L12-XX-AV	12.0V		78L12/XXxxx
OSU78L15-XX-AV	15.0V		78L15/XXxxx
OSU78L18-XX-AV	18.0V		78L18/XXxxx
OSU78L20-XX-AV	20.0V		78L20/XXxxx
OSU78L23-XX-AV	23.0V		78L23/XXxxx

Order Information

OSU78L①②-③④-AV

Designator	Symbol	Description
① ②	Integer	Output Voltage(3.3~23.0V)
③ ④	TE	Package: SOT23
	TS	Package: SOT89-3
	TT	Package: TO92

Block Diagram



Pin Configuration

SOT23 (Top View)

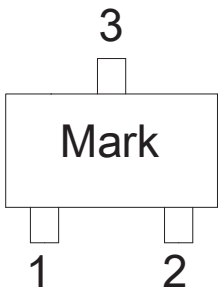


Table1: OSU78LXX series (SOT23 PKG)

PIN NO.	PIN NAME	FUNCTION
1	VOUT	Output voltage pin
2	VIN	Input voltage pin
3	GND	GND pin

SOT89 (Top View)

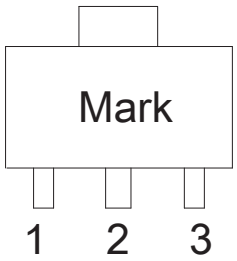


Table2: OSU78LXX series (SOT89-3 PKG)

PIN NO.	PIN NAME	FUNCTION
1	VOUT	Output voltage pin
2	GND	GND pin
3	VIN	Input voltage pin

TO92 (Top View)

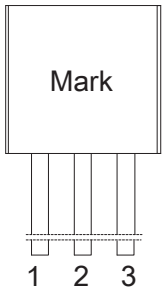


Table3: OSU78LXX series (TO92 PKG)

PIN NO.	PIN NAME	FUNCTION
1	VOUT	Output voltage pin
2	GND	GND pin
3	VIN	Input voltage pin

Absolute Maximum Ratings（Ta=25℃）

Parameter		Rating	Unit
Input supply voltage: VIN MAX		35	V
Output current: Iout MAX		150	mA
MAX Power: Pmax	SOT23	0.2	W
	SOT89	0.5	W
	TO92	0.5	W
Junction temperature: Tj		-55~150	℃
Operation temperature: Topr		-40~125	℃
Storage temperature: Tstr		-55~150	℃
Soldering temperature and time		+260(Recommended 10S)	℃
ESD Rating, (HBM)		5	KV

Note: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Electrical Characteristics

OSU78L33 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=8.3V	3.234	3.3	3.366	V
		Io=1mA~40mA VIN=5.3V~18V	3.135	3.3	3.465	
Line Regulation	LNR	VIN=8.3V~18V, Io=20mA	-20	-	20	mV
Load Regulation	LDR	VIN=8.3V, Io=1mA~100mA	-50	-	50	mV
		VIN=8.3V, Io=1mA~40mA	-30	-	30	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=6.3V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=8.3V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=6.3V~20V, I_O=1mA	-1.5	-	1.5	mA
		VIN=8.3V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L05 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=10V	4.9	5.0	5.1	V
		Io=1mA~40mA VIN=7V~18V	4.75	5.0	5.25	
Line Regulation	LNR	VIN=7V~18V, Io=20mA	-20	-	20	mV
Load Regulation	LDR	VIN=10V, Io=1mA~100mA	-50	-	50	mV
		VIN=10V, Io=1mA~40mA	-30	-	30	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=8V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=10V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=8V~20V, I_O=1mA	-1.5	-	1.5	mA
		VIN=10V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L06 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=11V	5.88	6.0	6.12	V
		Io=1mA~40mA VIN=8V~20V	5.7	6.0	6.3	
Line Regulation	LNR	VIN=8V~20V, Io=20mA	-30	-	30	mV
Load Regulation	LDR	VIN=11V, Io=1mA~100mA	-60	-	60	mV
		VIN=11V, Io=1mA~40mA	-40	-	40	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=9V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=11V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=9V~20V, I_O=1mA	-1.5	-	1.5	mA
		VIN=11V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L08 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=13V	7.84	8.0	8.16	V
		Io=1mA~40mA VIN=10V~23V	7.6	8.0	8.4	
Line Regulation	LNR	VIN=10V~23V, Io=20mA	-40	-	40	mV
Load Regulation	LDR	VIN=13V, Io=1mA~100mA	-65	-	65	mV
		VIN=13V, Io=1mA~40mA	-45	-	45	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=11V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=13V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=11V~23V, I_O=1mA	-1.5	-	1.5	mA
		VIN=13V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L09 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=14V	8.82	9.0	9.18	V
		Io=1mA~40mA VIN=11V~24V	8.55	9.0	9.45	
Line Regulation	LNR	VIN=11V~24V, Io=20mA	-40	-	40	mV
Load Regulation	LDR	VIN=14V, Io=1mA~100mA	-65	-	65	mV
		VIN=14V, Io=1mA~40mA	-45	-	45	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=12V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=14V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=12V~24V, I_O=1mA	-1.5	-	1.5	mA
		VIN=14V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L10 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=14V	9.8	10.0	10.2	V
		Io=1mA~40mA VIN=11V~24V	9.5	10.0	10.5	
Line Regulation	LNR	VIN=11V~24V, Io=20mA	-40	-	40	mV
Load Regulation	LDR	VIN=14V, Io=1mA~100mA	-65	-	65	mV
		VIN=14V, Io=1mA~40mA	-45	-	45	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=12V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=14V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=12V~24V, I_O=1mA	-1.5	-	1.5	mA
		VIN=14V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L12 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=17V	11.76	12.0	12.24	V
		Io=1mA~40mA VIN=14V~27V	11.4	12.0	12.6	
Line Regulation	LNR	VIN=14V~27V, Io=20mA	-50	-	50	mV
Load Regulation	LDR	VIN=17V, Io=1mA~100mA	-70	-	70	mV
		VIN=17V, Io=1mA~40mA	-50	-	50	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=17V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=17V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=14V~27V, I_O=1mA	-1.5	-	1.5	mA
		VIN=17V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L15 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=20V	14.7	15.0	15.3	V
		Io=1mA~40mA VIN=17V~30V	14.25	15.0	15.75	
Line Regulation	LNR	VIN=17V~30V, Io=20mA	-50	-	50	mV
Load Regulation	LDR	VIN=20V, Io=1mA~100mA	-70	-	70	mV
		VIN=20V, Io=1mA~40mA	-50	-	50	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=17V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=20V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=17V~30V, I_O=1mA	-1.5	-	1.5	mA
		VIN=20V, IOUT=1mA~40mA	-1	-	1	

LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

OSU78L18 (Cin=0.33uF, Co=0.1uF, Ta=25℃，unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout	Io=40mA, VIN=23V	17.64	18.0	18.36	V
		Io=1mA~40mA VIN=20V~28V	17.1	18.0	18.9	
Line Regulation	LNR	VIN=20V~28V, Io=20mA	-150	-	150	mV
Load Regulation	LDR	VIN=23V, Io=1mA~100mA	-170	-	170	mV
		VIN=23V, Io=1mA~40mA	-150	-	150	
Dropout Voltage	V_{DIF}	Ta=25℃，Io=100mA	-	2	-	V
Ripple Rejection	PSRR	Ta=25℃，f=120Hz, Io=10mA, VIN=23V	-	70	-	dB
Output noise Voltage	V_N	F=10Hz to 100KHz	-	40	-	uV/Vo
Quiescent Current	I_Q	VIN=23V, IOUT=40mA	-	1.7	-	mA
Quiescent Current Change	$\triangle I_Q$	VIN=20V~28V, I_O=1mA	-1.5	-	1.5	mA
		VIN=17V, IOUT=1mA~40mA	-1	-	1	

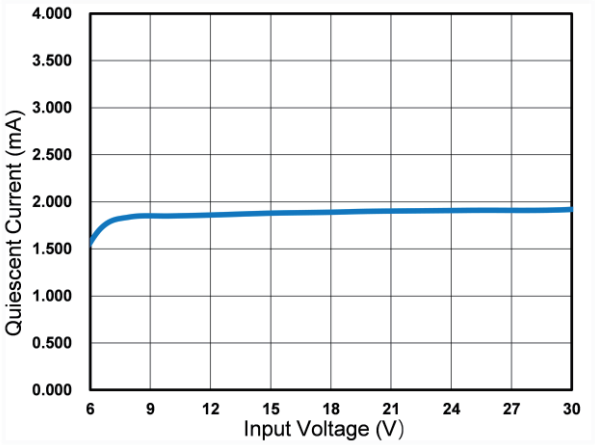
LNR: Line Regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

LDR: Load Regulation. The change in output voltage for a change in load current at constant chip temperature.

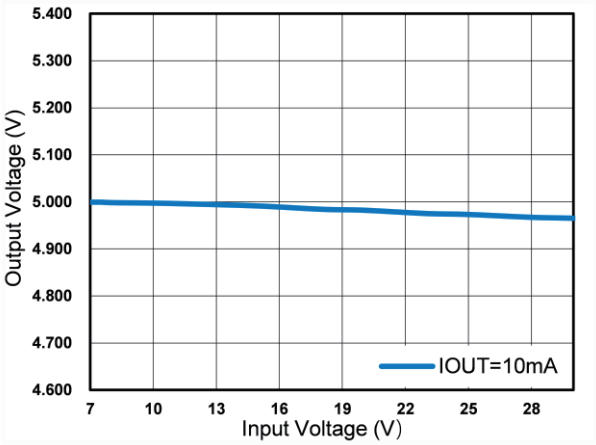
Typical Performance Characteristics

OSU78L05 (Note: C_{IN}=0.33uF, C_{OUT}=0.1μF, T=25℃, unless specified otherwise)

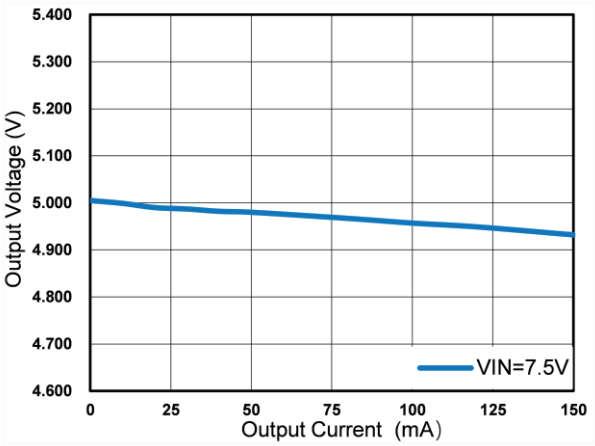
(1) Quiescent Current VS Input Voltage



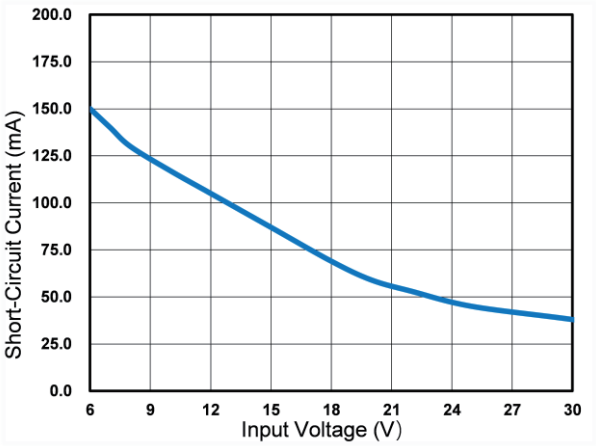
(2) Output Voltage VS Input Voltage



(3) Output Voltage VS Output Current

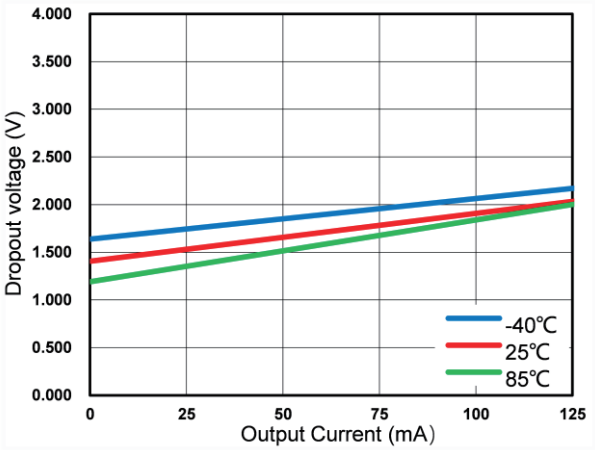


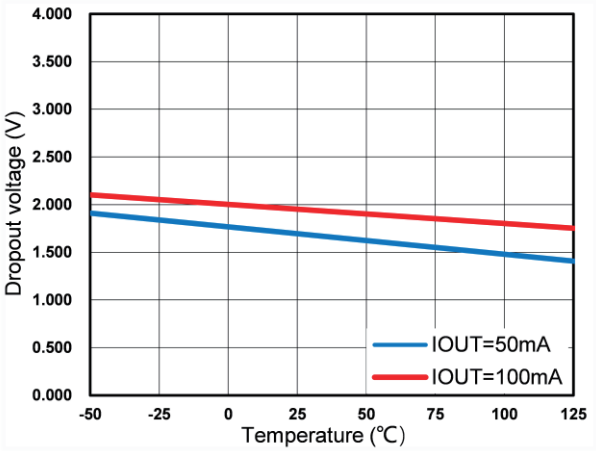
(4) Short-Circuit Current VS Input Voltage



(5) Dropout Voltage VS Output Current

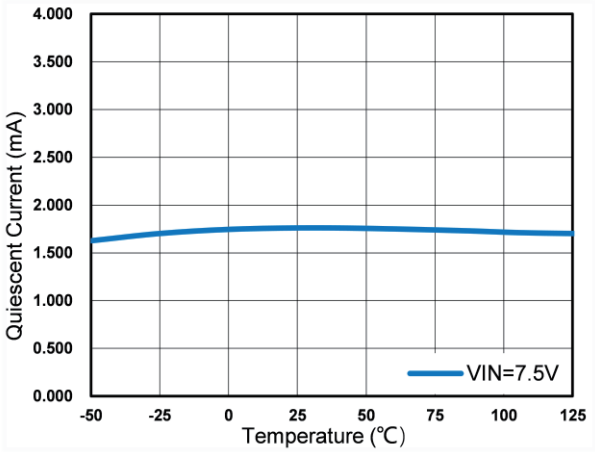
(6) Dropout Voltage VS Temperature

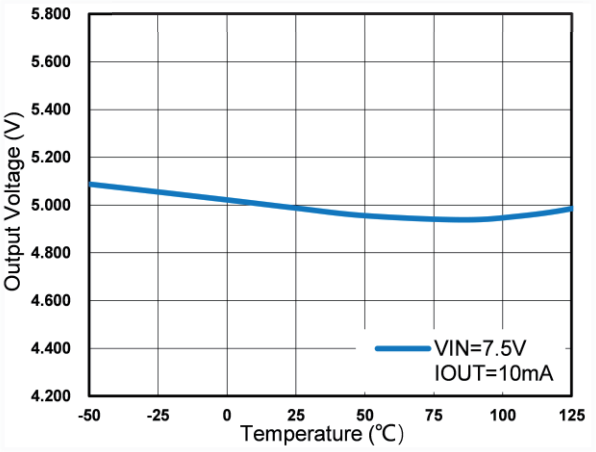




(7) Quiescent Current VS Temperature

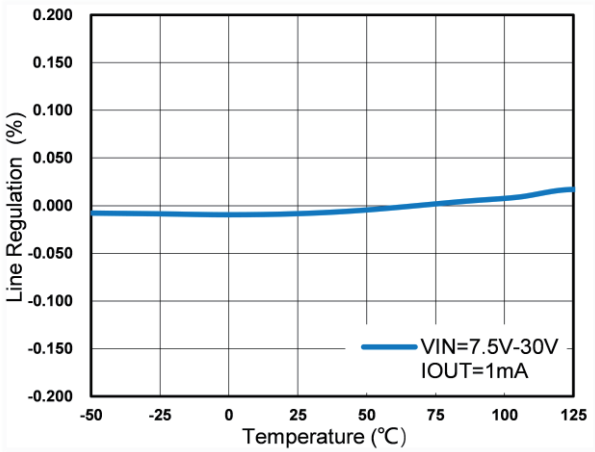
(8) Output Voltage VS Temperature

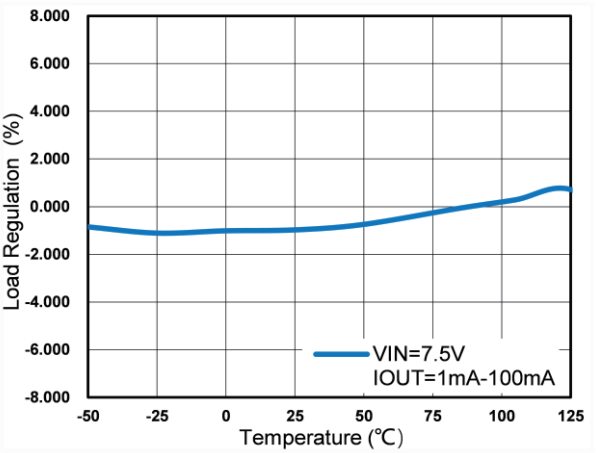




(9) Line Regulation VS Temperature

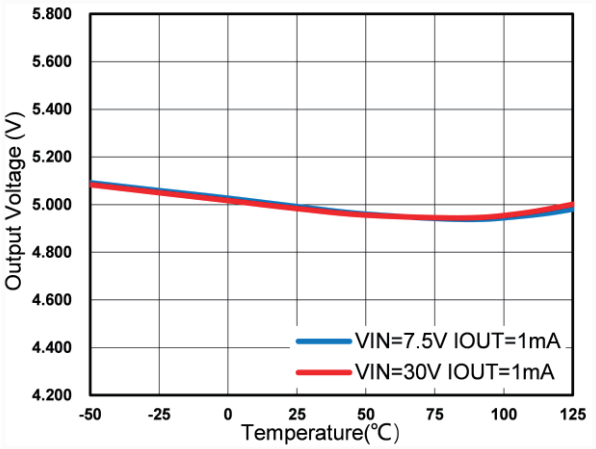
(10) Load Regulation VS Temperature

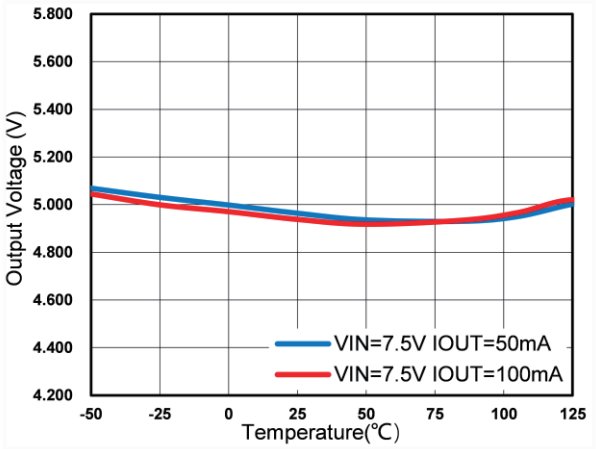




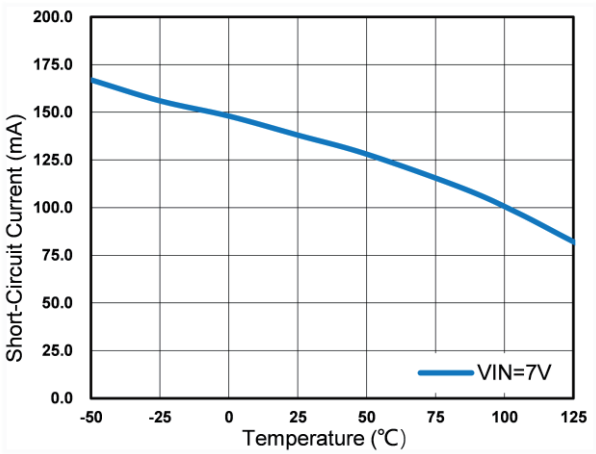
(11) Output Voltage VS Temperature

(12) Output Voltage VS Temperature

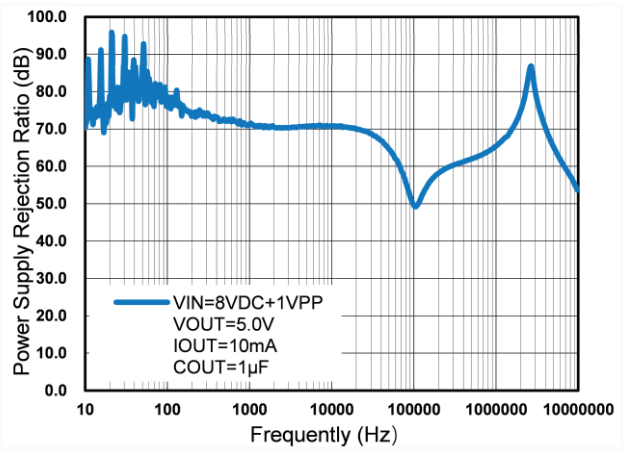




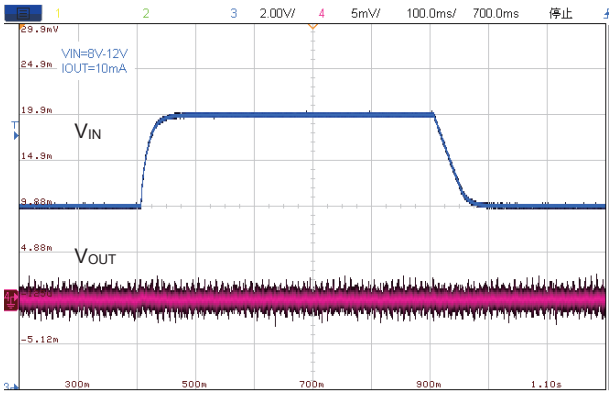
(13) Short-Current VS Temperature



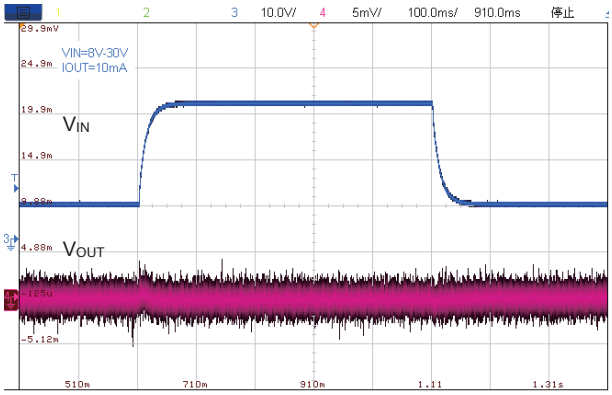
(14) PSRR



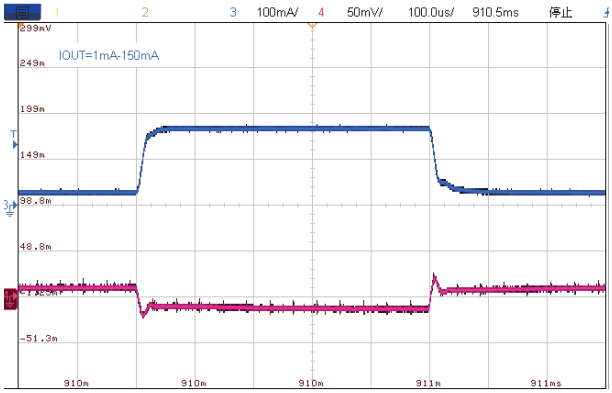
(15) Input Transient Response (VIN=8V-12V)



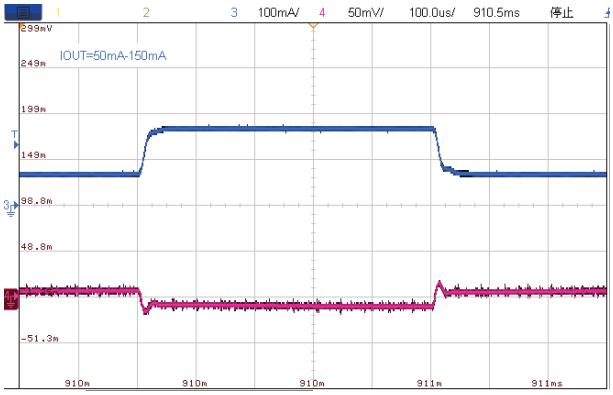
(16) Input Transient Response (VIN=8V-30V)



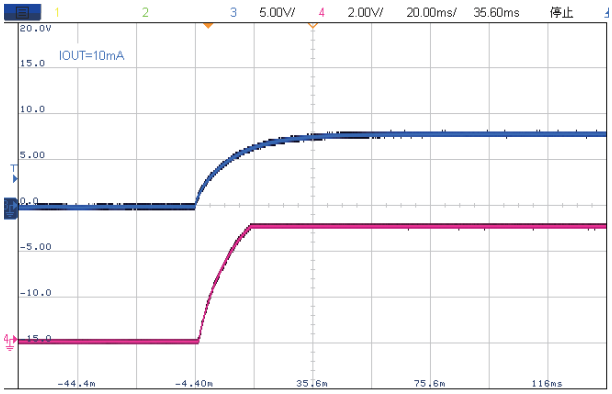
(17) Load Transient Response (IOUT=1mA-150mA)



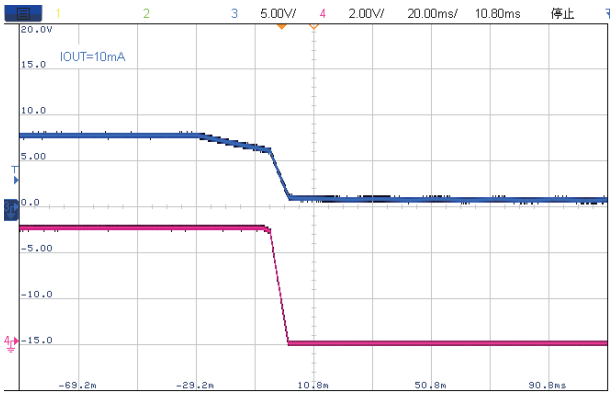
(18) Load Transient Response (IOUT=50mA-150mA)



(19) Power ON



(20) Power OFF



Operation Description

OSU78LXX-AV is designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Typical Application

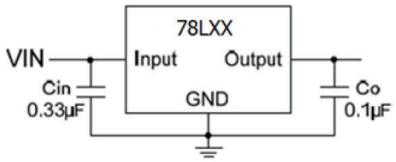


Fig.1 Typical Application

A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

Cin is required if regulator is located an appreciable distance from power supply filter.

Co is not needed for stability, however, it does improve transient response.

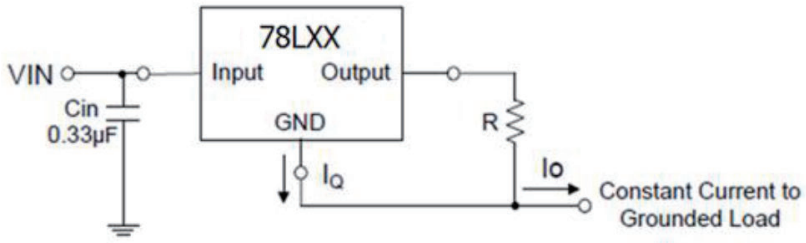
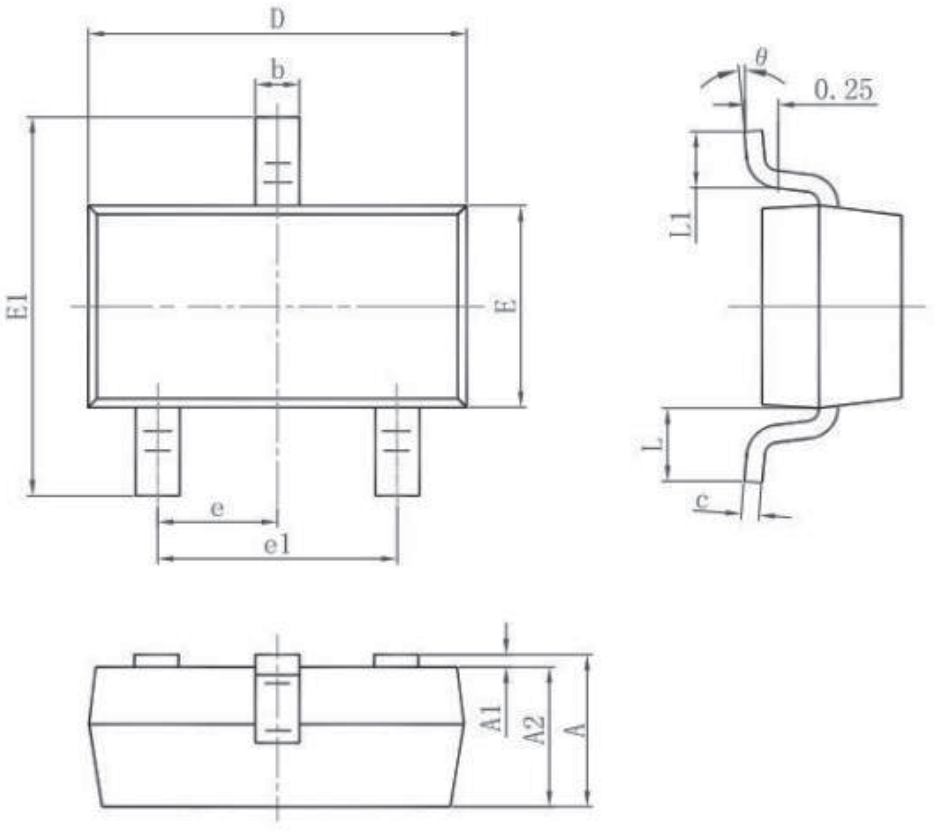


Fig.2 Constant Current Regulator

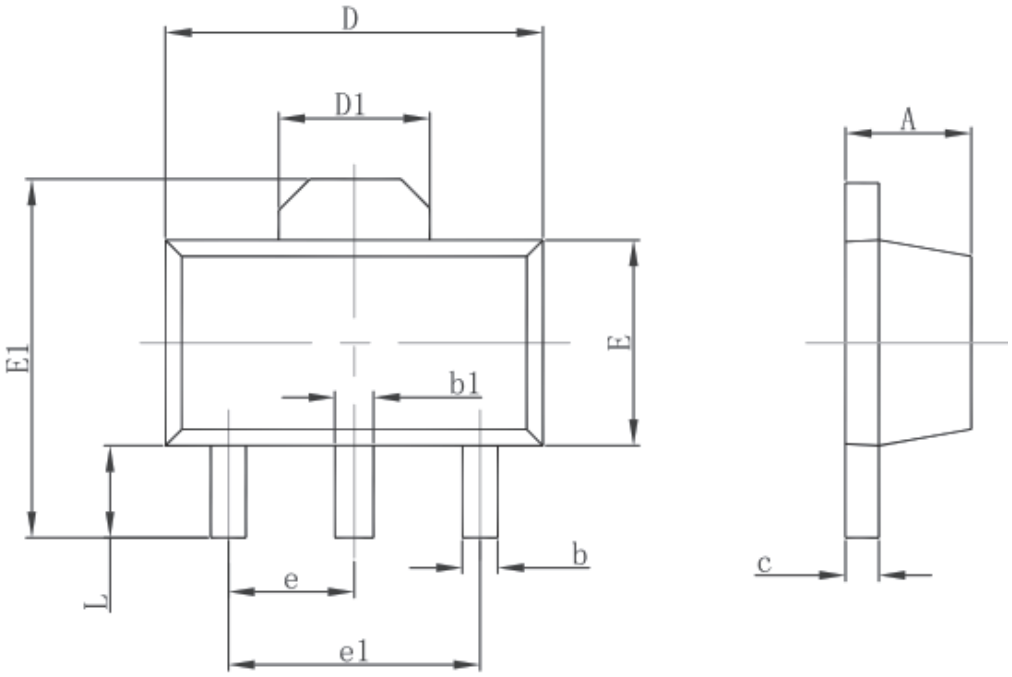
Package Information

3-pin SOT23 Outline Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

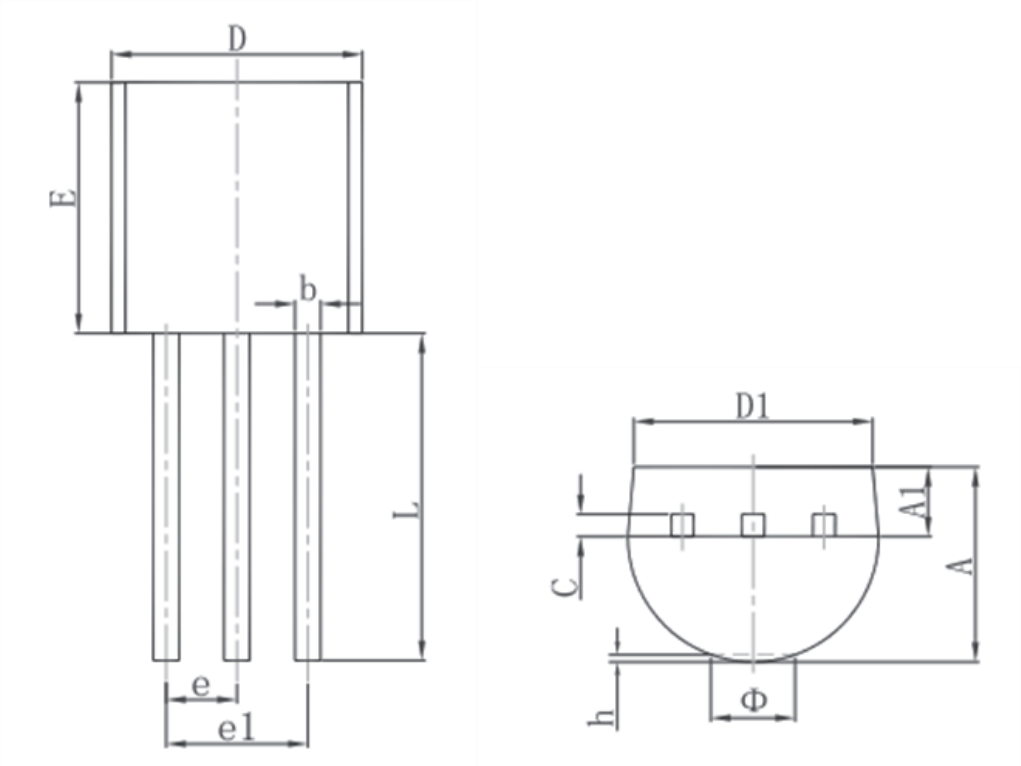


3-pin SOT89-3 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

3-pin TO92 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
D1	3.430		0.135	
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571
Φ		1.600		0.063
h	0.000	0.380	0.000	0.015

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