

General Description

FSMOS[®] MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially designed to use in motor control systems with driving voltage of more than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

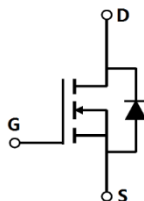
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$I_{D, pulse}$	800	A
$R_{DS(ON), max} @ V_{GS}=10V$	3	m Ω
Q_g	62	nC

Marking Information

Product Name	Package	Marking
SFS10R03UGNF	PDFN5 \times 6	SFS10R03UGN

Package & Pin information



Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_D	230	A
Pulsed drain current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{D, pulse}$	800	A
Continuous diode forward current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_S	230	A
Diode pulsed current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{S, pulse}$	800	A
Power dissipation ³⁾ , $T_C=25^{\circ}\text{C}$	P_D	250	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	240	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 175	$^{\circ}\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.59	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^{\circ}\text{C/W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{ V}, I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2		4	V	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		2.3	3	m Ω	$V_{GS}=10\text{ V}, I_D=30\text{A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}$
Gate resistance	R_G		2.4		Ω	$f=1\text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		4190		pF	$V_{GS}=0\text{ V}$, $V_{DS}=25\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		2150		pF	
Reverse transfer capacitance	C_{rss}		150		pF	
Turn-on delay time	$t_{d(on)}$		17		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\ \Omega$, $I_D=25\text{ A}$
Rise time	t_r		12		ns	
Turn-off delay time	$t_{d(off)}$		40		ns	
Fall time	t_f		14		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		62		nC	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $I_D=25\text{ A}$
Gate-source charge	Q_{gs}		17		nC	
Gate-drain charge	Q_{gd}		15		nC	
Gate plateau voltage	$V_{plateau}$		4.6		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		82		ns	$V_R=50\text{ V}$, $I_S=25\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		111		nC	
Peak reverse recovery current	I_{rrm}		2.7		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

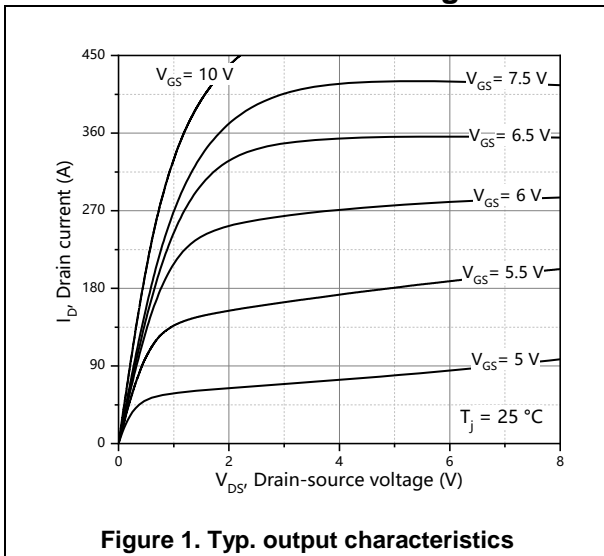


Figure 1. Typ. output characteristics

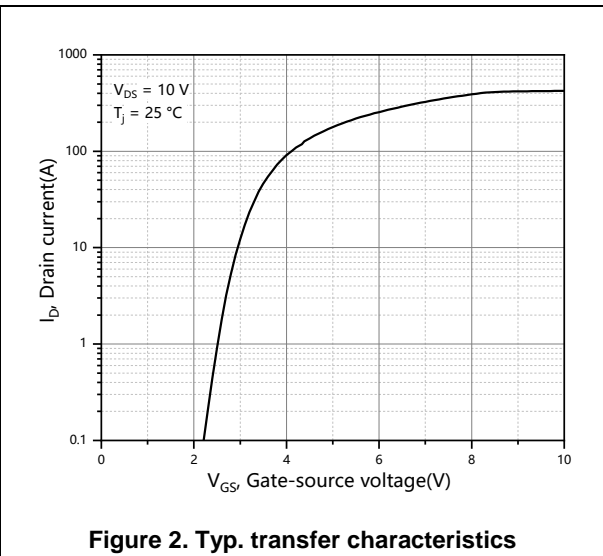


Figure 2. Typ. transfer characteristics

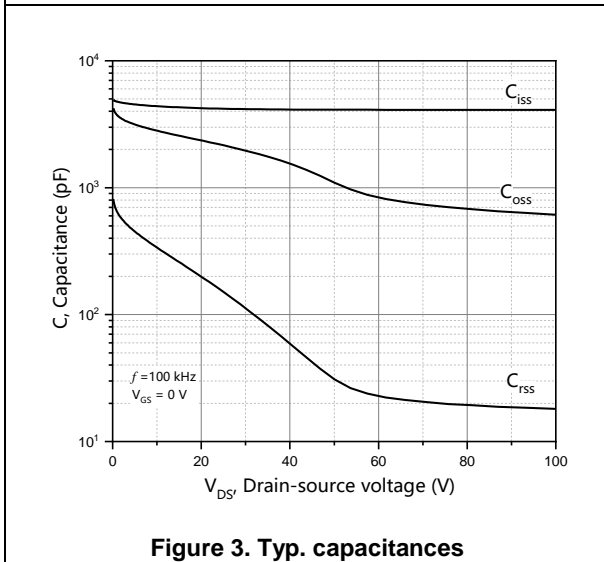


Figure 3. Typ. capacitances

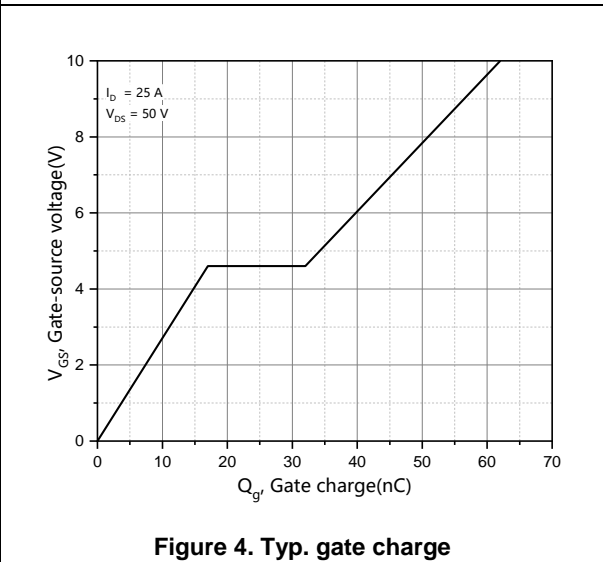


Figure 4. Typ. gate charge

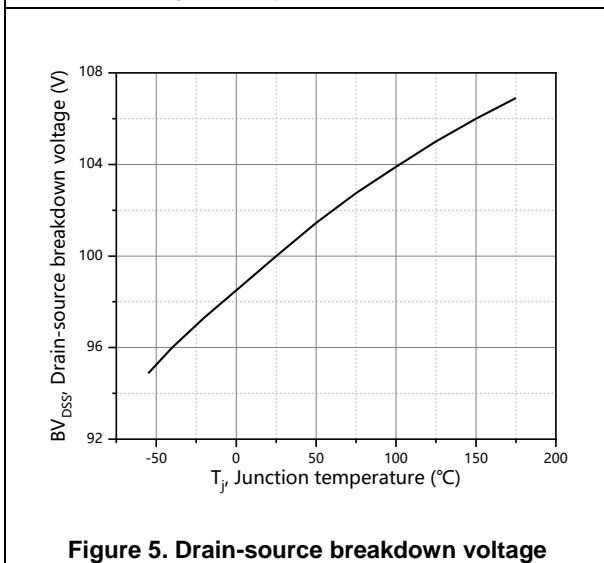


Figure 5. Drain-source breakdown voltage

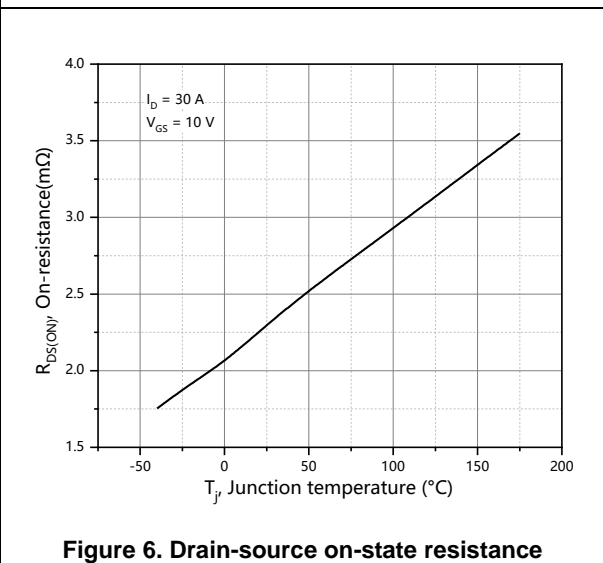


Figure 6. Drain-source on-state resistance

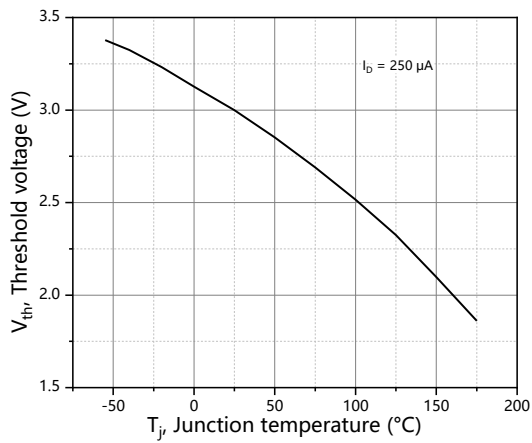


Figure 7. Threshold voltage

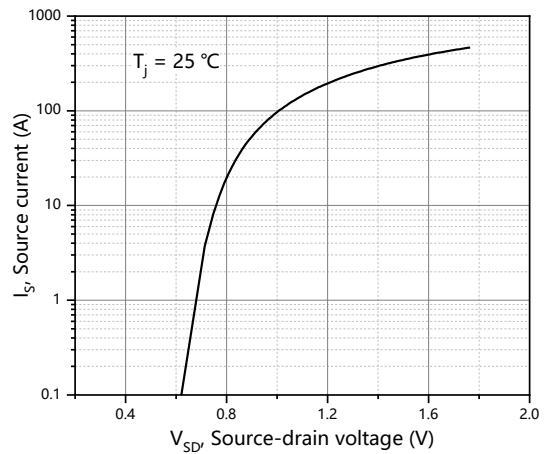


Figure 8. Forward characteristic of body diode

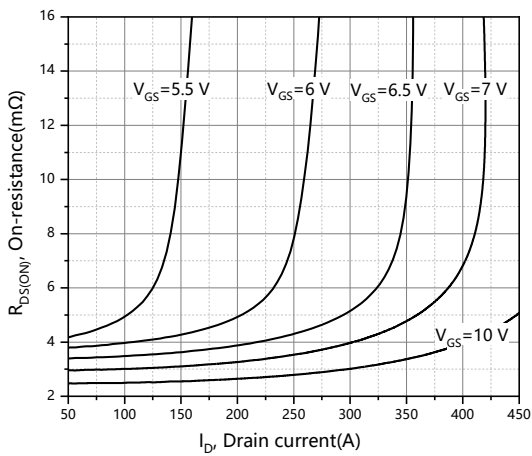


Figure 9. Drain-source on-state resistance

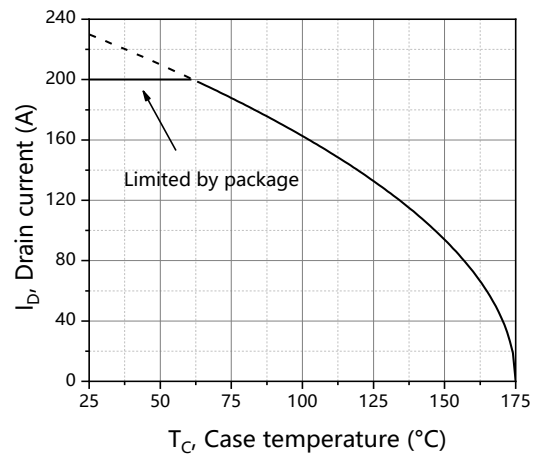


Figure 10. Drain current

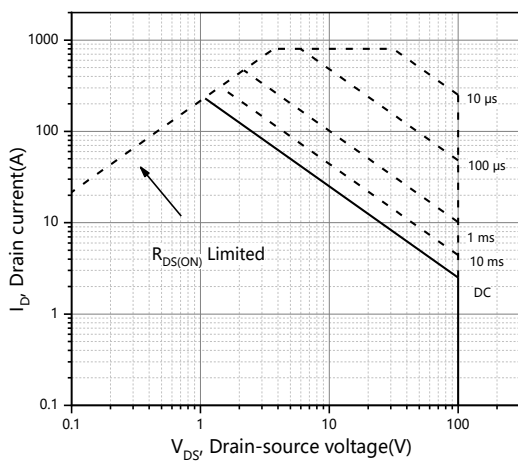


Figure 11. Safe operation area $T_c=25^\circ\text{C}$

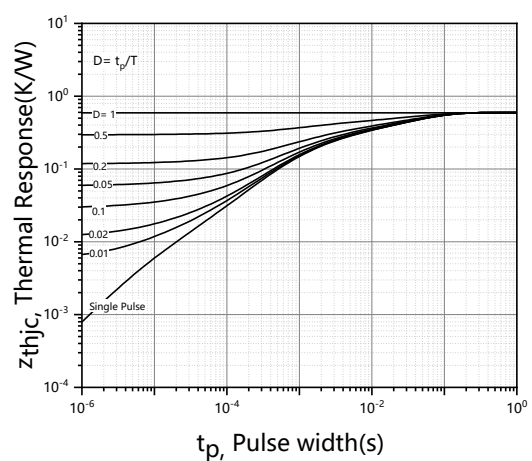


Figure 12. Max. transient thermal impedance

Test circuits and waveforms

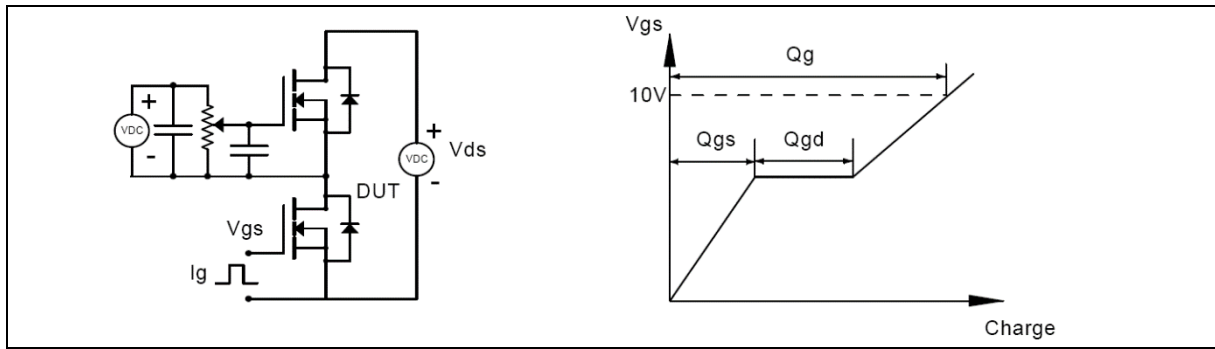


Figure 1. Gate charge test circuit & waveform

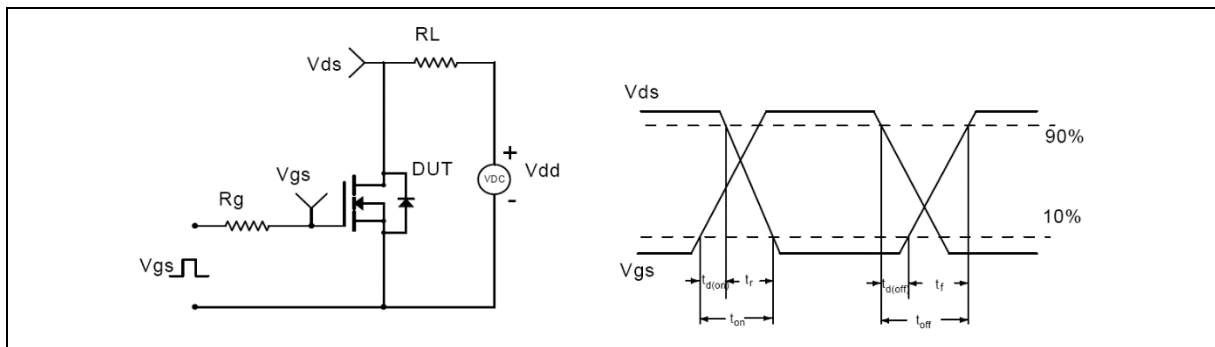


Figure 2. Switching time test circuit & waveforms

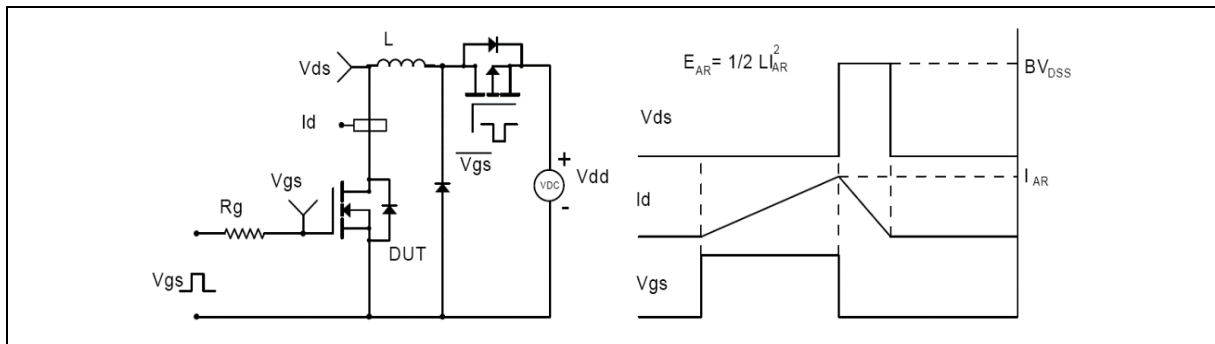


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

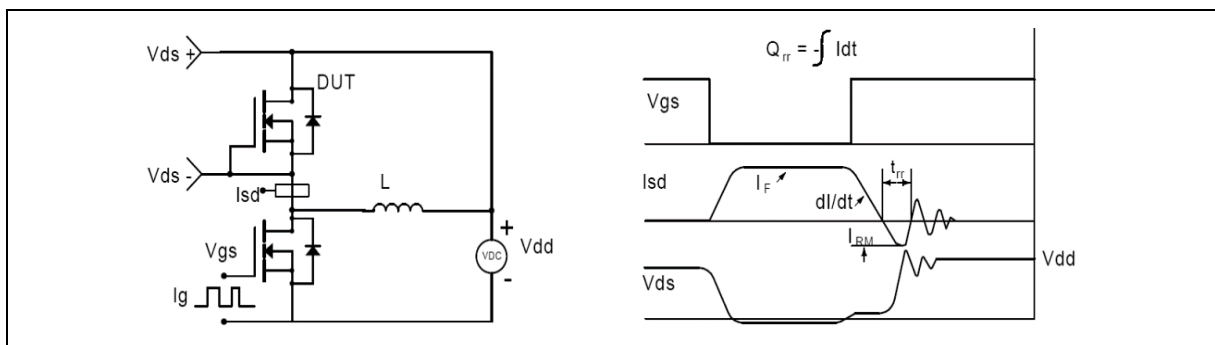
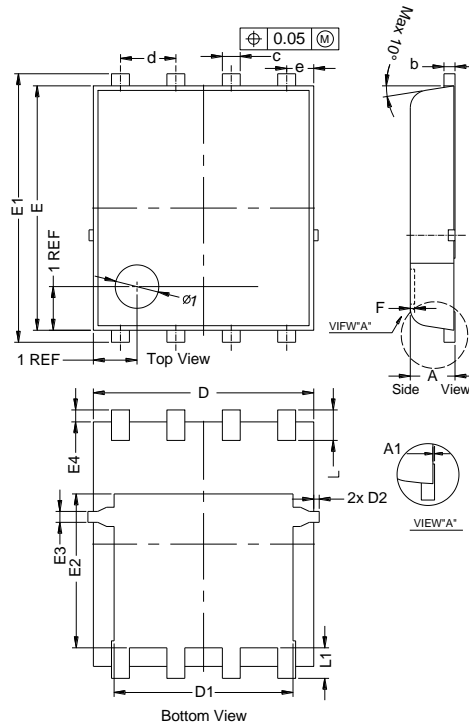


Figure 4. Diode reverse recovery test circuit & waveforms

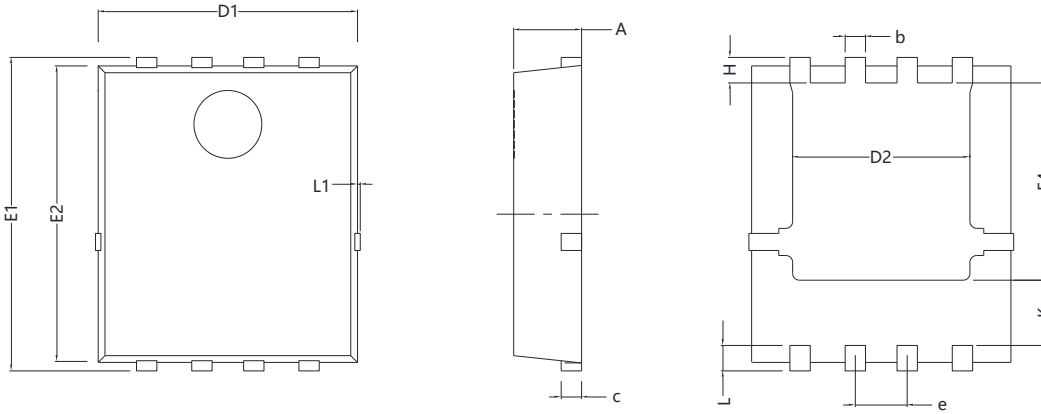
Package Information



Symbol	mm		
	Min	Nom	Max
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.246	0.254	0.312
c	0.31	0.41	0.51
d	1.27 BSC		
D	4.95	5.05	5.15
D1	4.00	4.10	4.20
D2	-	-	0.125
e	0.62 BSC		
E	5.50	5.60	5.70
E1	6.05	6.15	6.25
E2	3.425	3.525	3.625
E3	0.15	0.25	0.35
E4	0.175	0.275	0.375
F	-	-	0.10
L	0.50	0.60	0.70
L1	0.60	0.70	0.80
K	1.125	1.225	1.325

Version : PDFN5×6-H package outline dimension

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.05	5.25	5.45
D2	3.80	4.10	4.25
E1	5.95	6.15	6.35
E2	5.76	5.86	5.96
E4	3.90	4.10	4.30
e	1.27 BSC		
H	0.295	0.395	0.495
K	1.055 REF		
L	0.30	0.60	0.70
L1	0.01	0.05	0.12

Version : PDFN5*6-PL package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
PDFN5×6-H	5000	2	10000	5	50000
PDFN5×6-P	5000	2	10000	5	50000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS10R03UGNF	PDFN5×6	yes	yes	yes

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Revision History

Version	Revision History	Date
V1.0	Initial release	2023-07-24
V1.1	Add assembly site "P"	2025-07-25