General Description

FSMOS® MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially designed to use in motor control systems with driving voltage of more than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery

RoHS compliant

Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

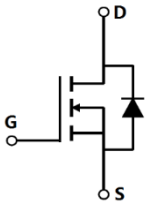
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$I_{D, pulse}$	800	A
$R_{DS(ON), max}$ @ V_{GS}=10V	2.3	mΩ
Q_g	85	nC

Marking Information

Product Name	Package	Marking
SFS08R023HNF	TO-247-3L	SFS08R023HN

Package & Pin information



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Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current[1], T_C=25 °C	I_D	210	A
Pulsed drain current[2], T_C=25 °C	$I_{D,\ pulse}$	800	A
Continuous diode forward current[1], T_C=25 °C	I_S	210	A
Diode pulsed current[2], T_C=25 °C	$I_{S,\ pulse}$	800	A
Power dissipation[3], T_C=25 °C	P_D	200	W
Single pulsed avalanche energy[4]	E_{AS}	375	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.62	°C/W
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	°C/W

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	80			V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	2		4	V	V_{DS}=V_{GS}, I_D=250 μA
Drain-source on-state resistance	$R_{DS(ON)}$		2	2.3	mΩ	V_{GS}=10 V, I_D=50 A
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=20 V
				-100		V_{GS}=-20 V
Drain-source leakage current	I_{DSS}			1	μA	V_{DS}=80 V, V_{GS}=0 V
Gate resistance	R_G		2		Ω	f=1 MHz, Open drain

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Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		6510		pF	V_{GS}=0 V, V_{DS}=25 V, f=100 kHz
Output capacitance	C_{oss}		3250		pF	
Reverse transfer capacitance	C_{rss}		178		pF	
Turn-on delay time	$t_{d(on)}$		22		ns	V_{GS}=10 V, V_{DS}=40V, R_G=2 Ω, I_D=50 A
Rise time	t_r		13		ns	
Turn-off delay time	$t_{d(off)}$		45		ns	
Fall time	t_f		16		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		85		nC	V_{GS}=10 V, V_{DS}=40V, I_D=50 A
Gate-source charge	Q_{gs}		24		nC	
Gate-drain charge	Q_{gd}		17		nC	
Gate plateau voltage	$V_{plateau}$		4.1		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	I_S=12 A, V_{GS}=0 V
Reverse recovery time	t_{rr}		95		ns	V_R=40 V, I_S=50 A, di/dt=100 A/μs
Reverse recovery charge	Q_{rr}		168		nC	
Peak reverse recovery current	I_{rrm}		3.4		A	

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) V_{DD}=50V,V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

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Electrical Characteristics Diagrams

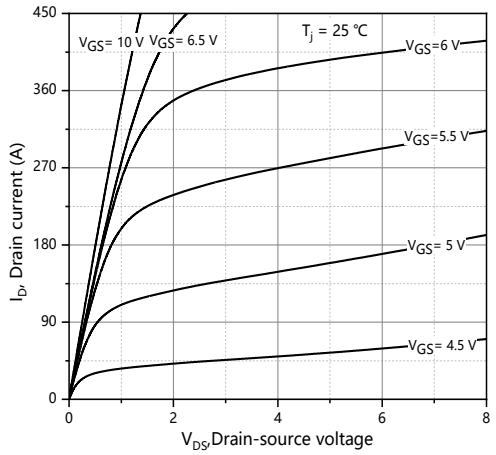

Figure 1. Typ. output characteristics

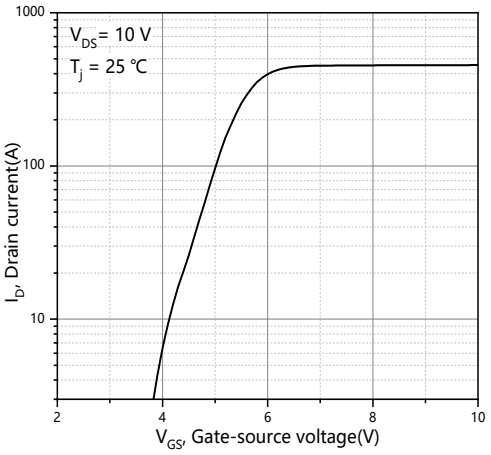

Figure 2. Typ. transfer characteristics

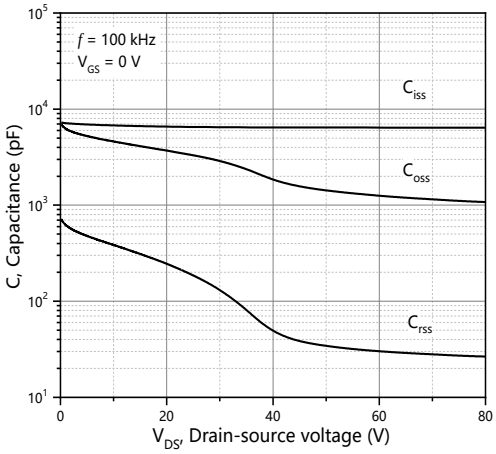

Figure 3. Typ. capacitances

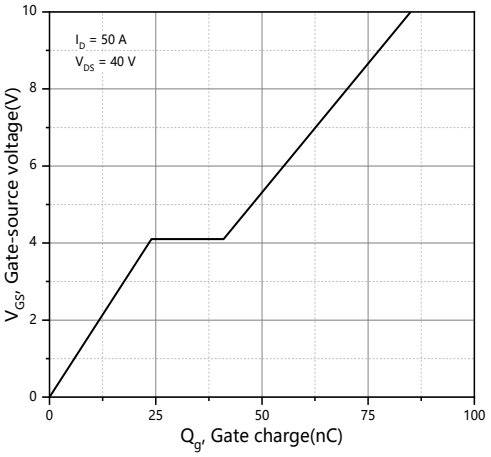

Figure 4. Typ. gate charge

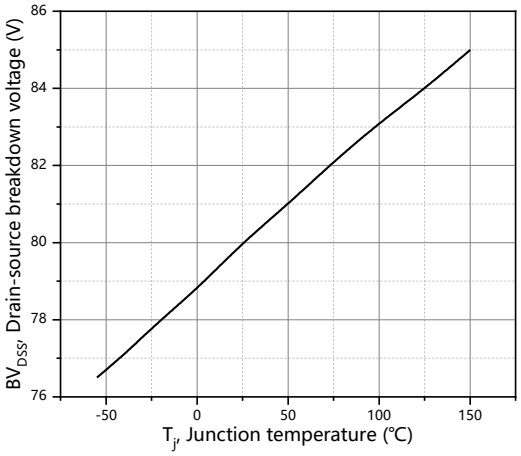

Figure 5. Drain-source breakdown voltage

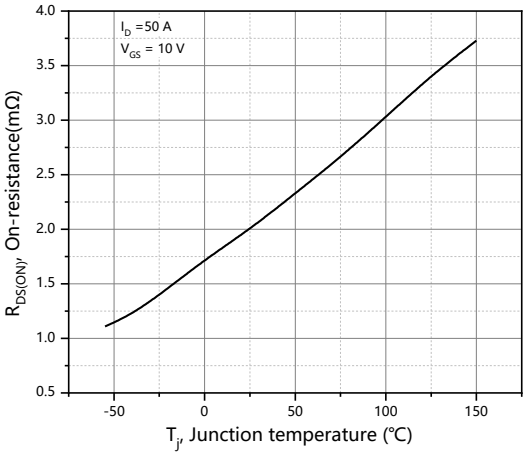

Figure 6. Drain-source on-state resistance

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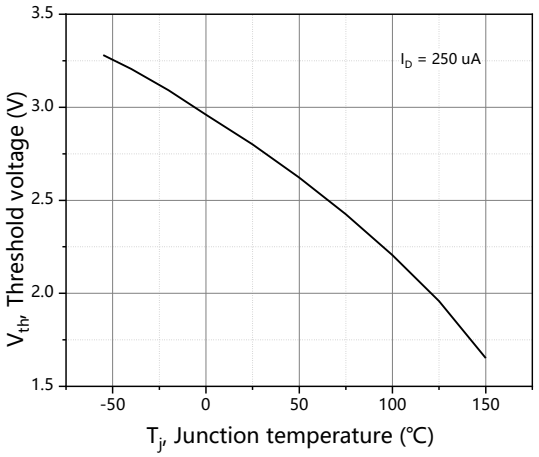

Figure 7. Threshold voltage

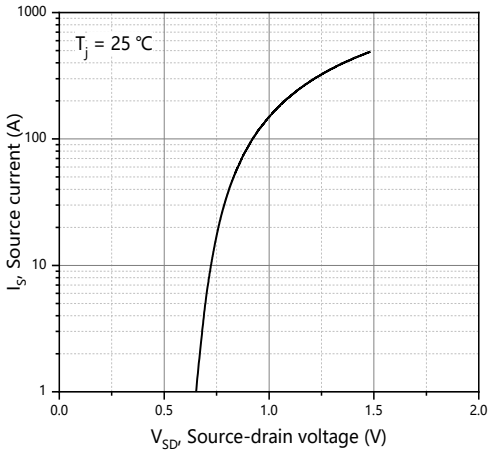

Figure 8. Forward characteristic of body diode

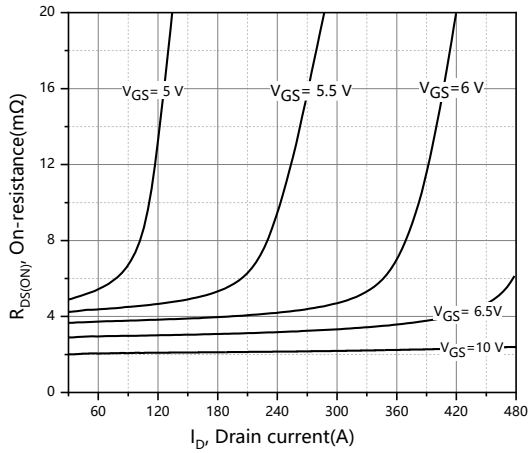

Figure 9. Drain-source on-state resistance

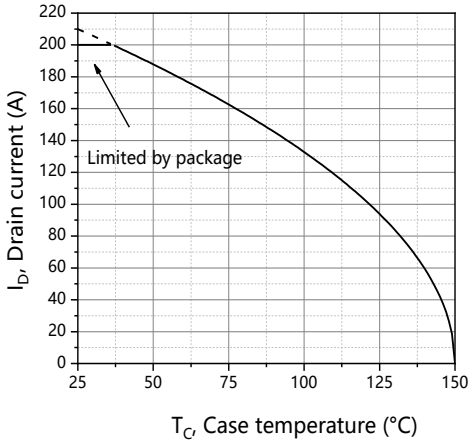

Figure 10. Drain current

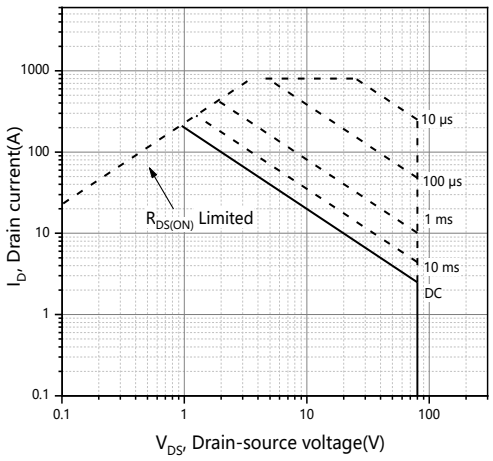

Figure 11. Safe operation area T_C=25℃

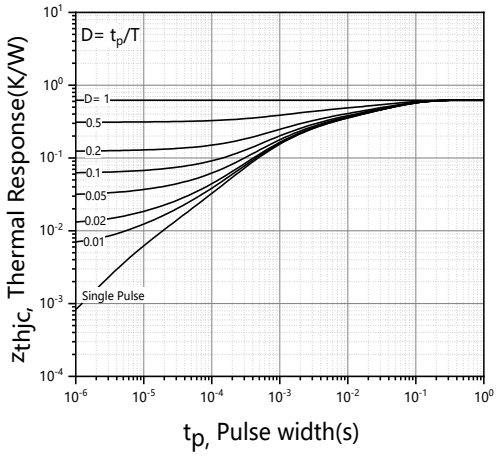

Figure 12. Max. transient thermal impedance

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Test circuits and waveforms

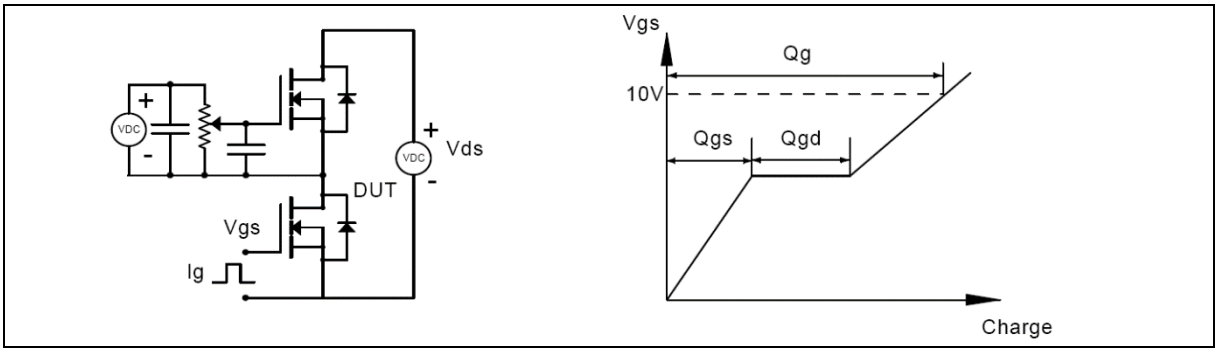


Figure 1. Gate charge test circuit & waveform

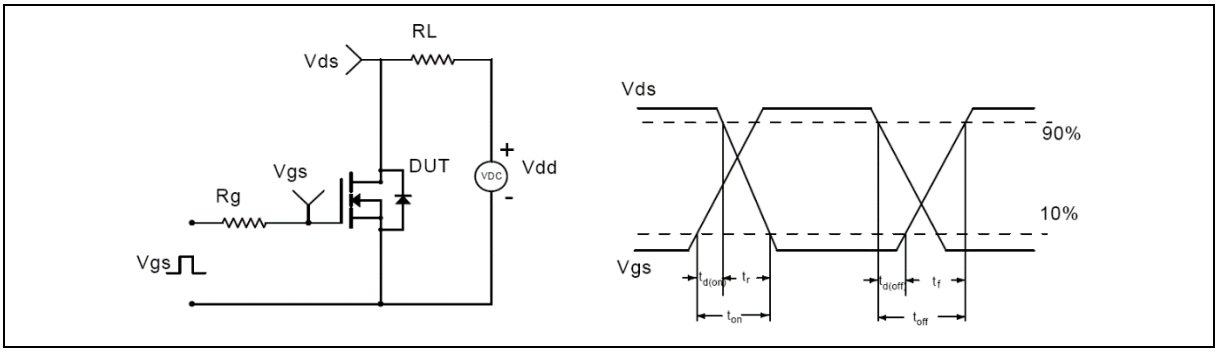


Figure 2. Switching time test circuit & waveforms

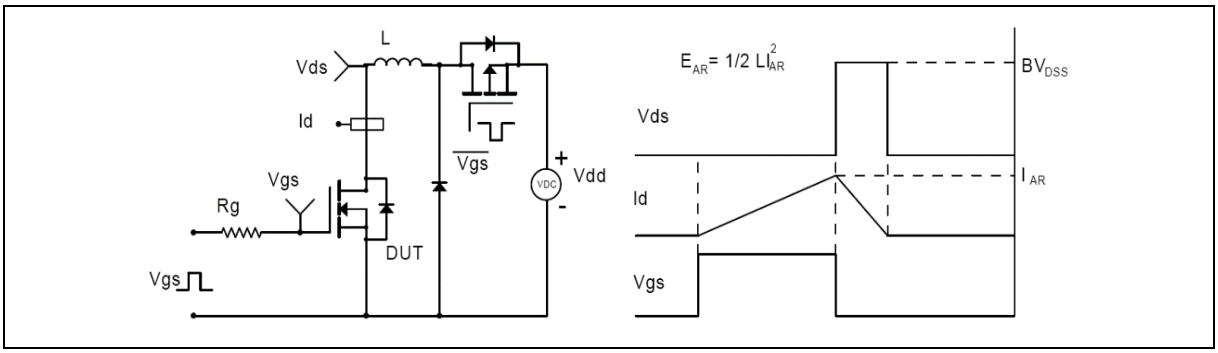


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

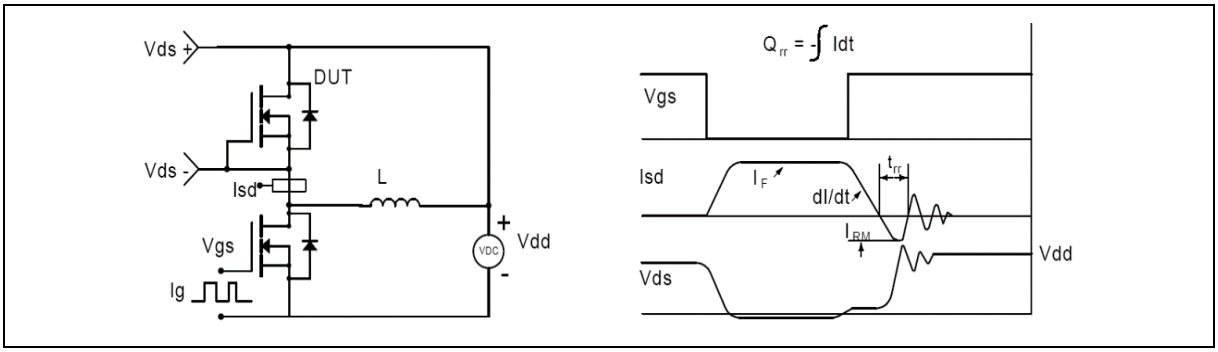
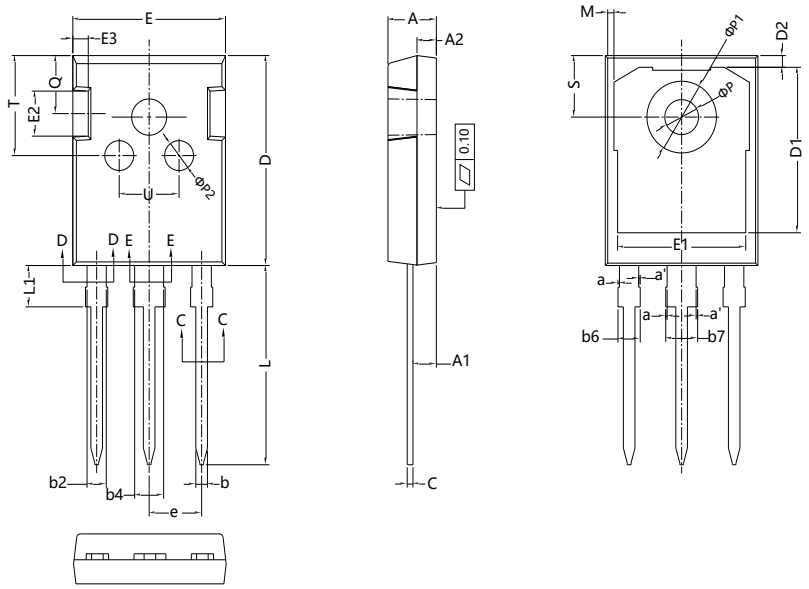


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
a	0.00	-	0.15
a'	0.00	-	0.15
b	1.16	-	1.26
b2	1.96	-	2.06
b4	2.96	-	3.06
b6	-	-	2.25
b7	-	-	3.25
c	0.59	-	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.17	1.35
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.40	4.50	4.60
E3	1.50	1.60	1.70
e	5.436 BSC		
L	19.80	19.92	20.10
L1	-	-	4.30
M	0.35	-	0.95
P	3.40	3.50	3.60
P1	7.00	-	7.40
P2	2.40	2.5	2.6
Q	5.60	-	6.0
S	6.05	6.15	6.25
T	9.8	-	10.20
U	6.00	-	6.40

Version 1: TO-247-3L-J package outline dimension

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Ordering Information

Package Type	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO-247-3L-J	30	20	600	4	2400

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS08R023HNF	TO-247-3L	yes	yes	yes

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Revision History

Version	Revision History	Date
V1.0	Initial release	2024-01-18

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