PWM Doubler Logic

HP1800

FEATURES

- Up to 7 V Supply Voltage
- Configurable Phase Multiplier as Doubler from A Single PWM Input
- Capable of Generating High Output Switching Frequency from 200 kHz to 2000 kHz
- Tri-State PWM Input for Power Stage Shutdown
- Small Size: DFN2x2-8L Package
- Operating Ambient Temperature Range of -40°C to 125°C

APPLICATIONS

Desktop Computers

Data Center

GENERAL DESCRIPTION

The OSU1800 is a phase multiplier which is designed to double the phase count from a controller.

The OSU1800 is capable of driving two independent power stages from a single PWM input. The input PWM signal is internally split to drive two power stages 180° out of phase, each at half of the PWM input frequency.

The OSU1800 is available in DFN-8L package, 2 mm x 2 mm body size.

TYPICAL APPLICATION CIRCUIT

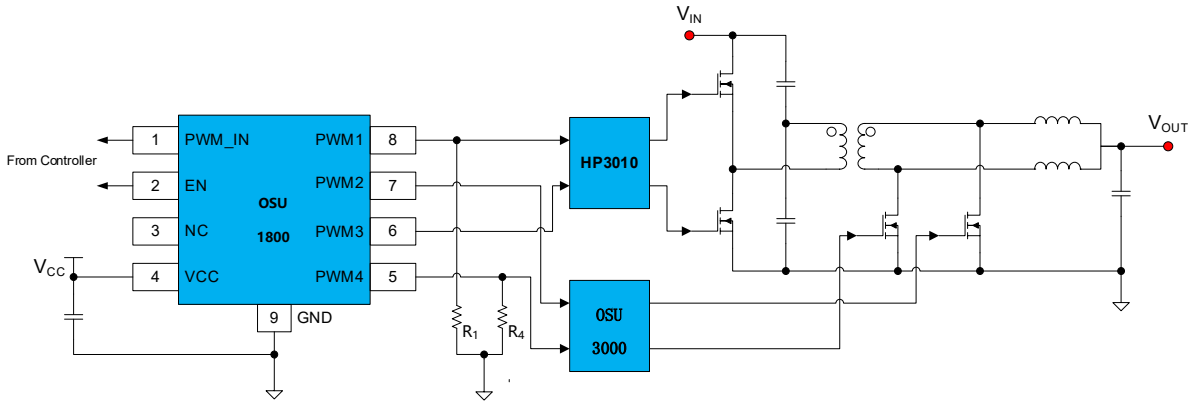

Figure 1 Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	08/14/2025	Initial version
Rev. 1.1	12/2025	Added details of PWM timing. Updated tri-state window in electrical specification.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

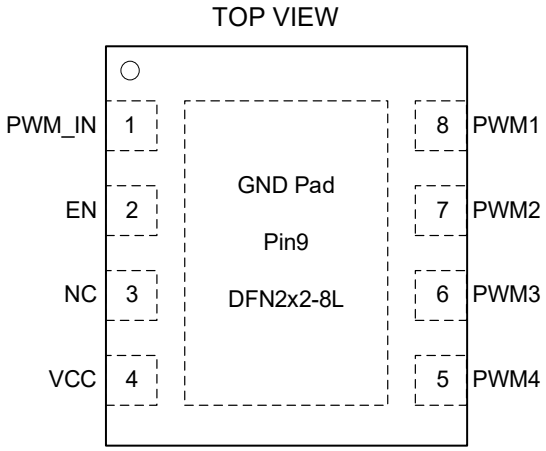


Figure 2 OSU1800-AA000-DN08R Pin Assignment

Table 1. Pin Function Descriptions for OSU1800-AA000-DN08R

Pin No.	Name	Function
1	PWM_IN	The PWM_IN is the control signal input. Connect this pin to the PWM output of the controller.
2	EN	Enable output PWM. This pin asserted LOW disables PWM output. This pin biased high enables all output PWM.
3	NC	No connection. It must be left unconnected.
4	VCC	Supply voltage.
5	PWM4	PWM4 signal to the power stage (Initialize the rising edge dead time).
6	PWM3	PWM3 signal to the power stage.
7	PWM2	PWM2 signal to the power stage.
8	PWM1	PWM1 signal to the power stage (Initialize the falling edge dead time).
9	GND	Reference ground. All signals are referenced to this node.

SPECIFICATIONS

VCC = 5 V to 7 V, T_A = -40°C to +125°C, unless otherwise specified.

Table 2. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC						
Supply Voltage			5		7	V
Supply Current	V_{ICC}	V_{CC} = 5 V, C_{PWM} = 50 pF, PWM_IN = 1 MHz, Duty = 50%; $R_{PWM1/4}$ = 3.3 kΩ; $R_{PWM2/3}$ = open			4	mA
UVLO Vcc Rising	V_{UVLO_R}		3.6	4.1	4.5	V
UVLO Vcc Falling	V_{UVLO_F}	PWM1/2/3/4 output voltage < 0.8 V	3.3	3.8	4.3	V
UVLO Hysteresis			0.1	0.3	0.5	V
UVLO Vcc Falling Delay		Measured from V_{CC} falling < 3.6 V to PWM1 < 0.8 V			1	μs
EN						
EN Input High Threshold	V_{EN_H}		2.4			V
EN Input Low Threshold	V_{EN_L}				0.8	V
Internal Pull-up Resistance	R_{PULLUP_EN}		10		300	kΩ
EN Floating Voltage	V_{EN_F}	VCC = 5 V to 7 V	2.7		3.4	V
Enable Power-on Delay	$t_{EN\_on\_delay}$	Measured from EN rising edge to PWM1 > 1 V			5	μs
Enable Power-off Delay	$t_{EN\_off\_delay}$	Measured from EN falling edge to PWM1 < 1 V			0.2	μs
PWM_IN						
PWM Voltage	V_{PWM_OP}		0		3.3	V
PWM Input High Threshold	V_{IH}	PWM low or Tri-state to high	2.6			V
PWM Input Low Threshold	V_{IL}	PWM high or Tri-state to low			0.75	V
Transition Time-Rise		Measured from 0.4 V to 2.9 V			15	ns
Transition Time-Fall		Measured from 2.9 V to 0.4 V			15	ns
Tri-state Window	V_{PWM_S}		1.2		1.95	V
PWM Hysteresis	V_{PWM_HYS}	Active to Tri-state or Tri-state to Active	1	40	120	mV
PWM Input Tri-State Floating Voltage	V_{PWM_TRI}		1.4	1.6	1.8	V
Internal Pull-up Resistance			3.3	10	20	kΩ
Internal Pull-down Resistance			3.3	10	20	kΩ
Frequency of The PWM Input	f_{SW}		0.2		2.0	MHz
Recognized PWM Pulse Width		T_{PRD} is the period of PWM_IN input signal	40		T_{PRD} - 40	ns
PWM1, PWM2, PWM3, PWM4						
PWM Output High Threshold	$V_{OH(PWM)}$	Load resistance to GND ≥ 3.3 kΩ	2.9	3.15	V_{CC} + 0.3	V
PWM Output Low Threshold	$V_{OL(PWM)}$				0.4	V
Transition Time-Rise	$T_{R(HS)}$	C_{PWM} = 50 pF, R_{PWM} = 3.3 kΩ, Measured from 0.4 V to 2.9 V			15	ns
Transition Time-Fall	$T_{F(HS)}$	C_{PWM} = 50 pF, measured from 2.9 V to 0.4 V			15	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation Delay-Enter Tri-State	$T_{PDTS(en)}$	Measured from the edge PWM_IN enters tri-state to PWM2/PWM 4 low			70	ns
Minimum Output Pulse Width	T_{MinPWM}				40	ns
Initialization Time		V_{CC} rises to PWM output time. PWM output low level before initialization finish			2	ms
PWM1 Voltage Before Initialization		Connect with 150 kΩ to GND			0.8	V
PWM2 Voltage Before Initialization		Floating			0.8	V
PWM3 Voltage Before Initialization		Floating			0.8	V
PWM4 Voltage Before Initialization		Connect with 150 kΩ to GND			0.8	V

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum ratings

Parameter	Rating
Supply voltage, VCC	-0.3 V to 8 V
PWM_IN, PWM1, PWM2, PWM3, PWM4, EN	-0.3 V to VCC + 0.3 V
Operating temperature range (Ambient)	-40 to +125°C
Operating temperature range (Junction)	-40 to +150°C
Storage temperature range	-55 to +150°C
Soldering conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human body model	±4000 V
Charged device model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extending periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to print circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
DFN2x2-8L	111.5	73.2	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5 V. T_A = -40°C to +125°C, unless otherwise specified.

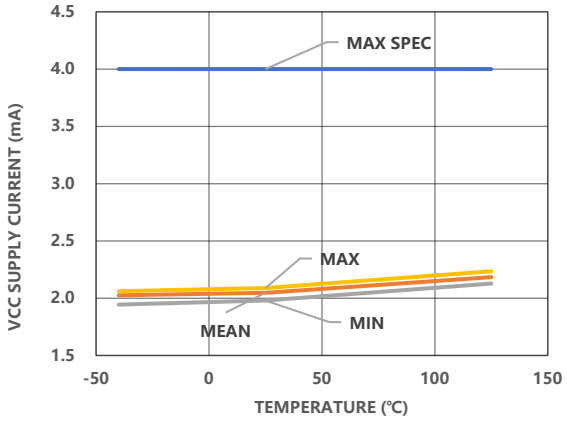


Figure 3 VCC Supply Current vs. Temperature

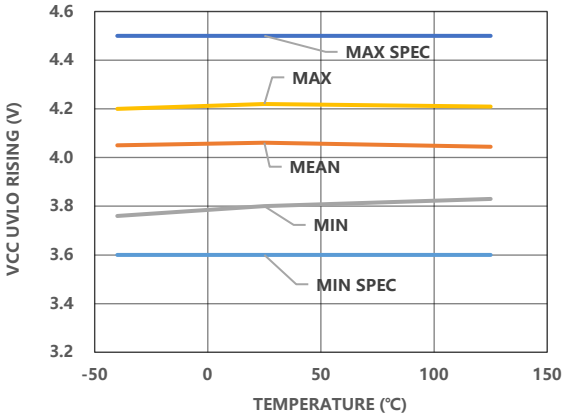


Figure 4 VCC UVLO Rising vs. Temperature

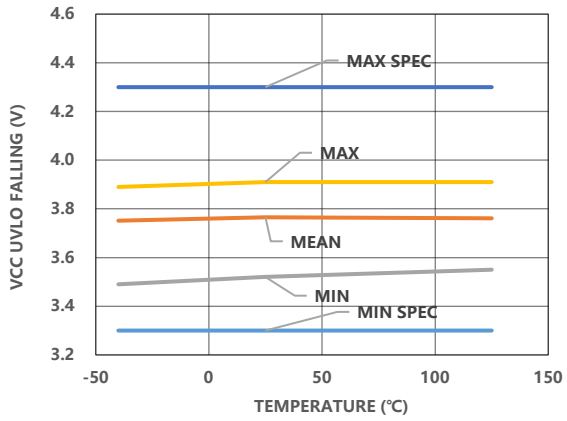


Figure 5 VCC UVLO Falling vs. Temperature

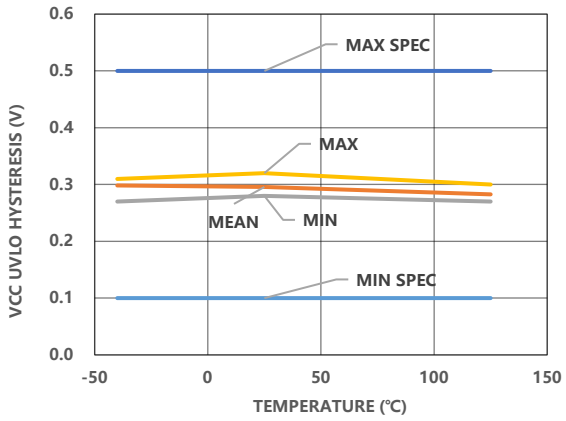


Figure 6 VCC UVLO Hysteresis vs. Temperature

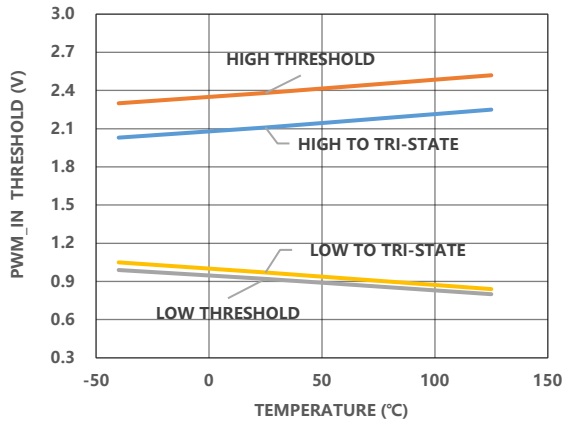


Figure 7 PWM_IN Threshold vs. Temperature

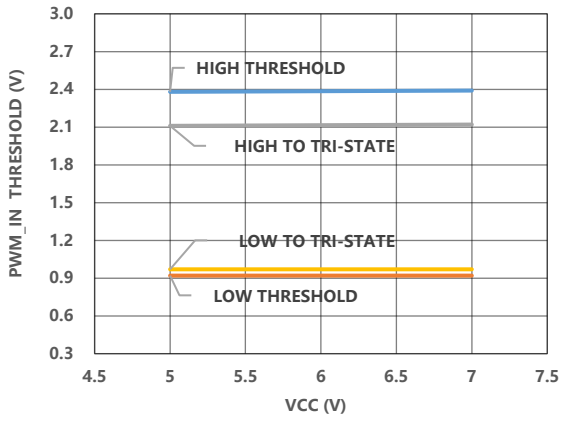


Figure 8 PWM_IN Threshold vs. VCC

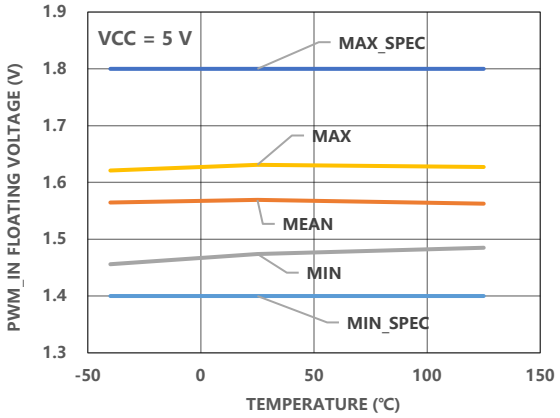


Figure 9 PWM_IN Floating Voltage vs. Temperature, VCC = 5 V

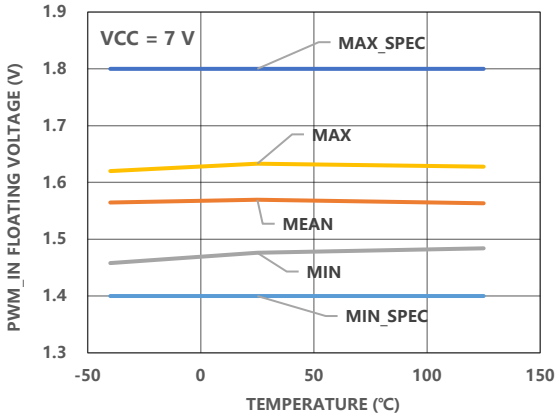


Figure 10 PWM_IN Floating Voltage vs. Temperature, VCC = 7 V

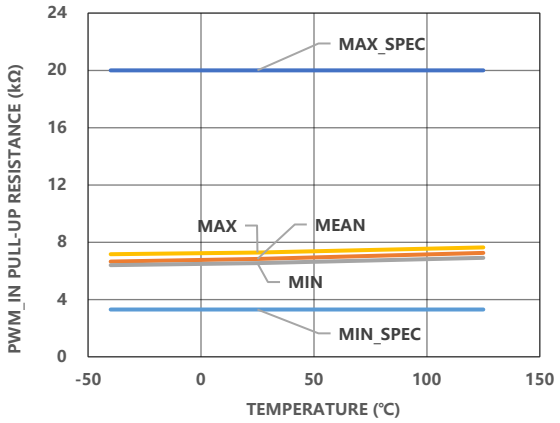


Figure 11 PWM_IN Pull-up Resistance vs. Temperature

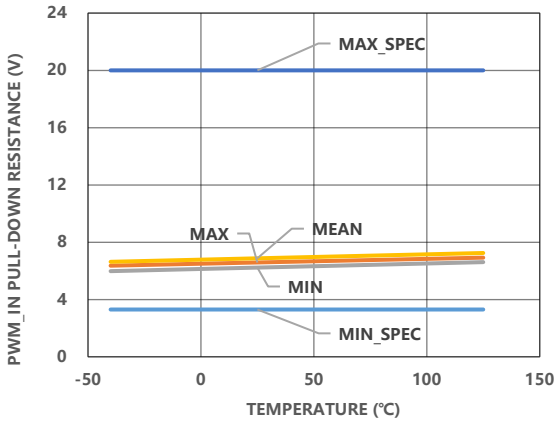


Figure 12 PWM_IN Pull-down Resistance vs. Temperature

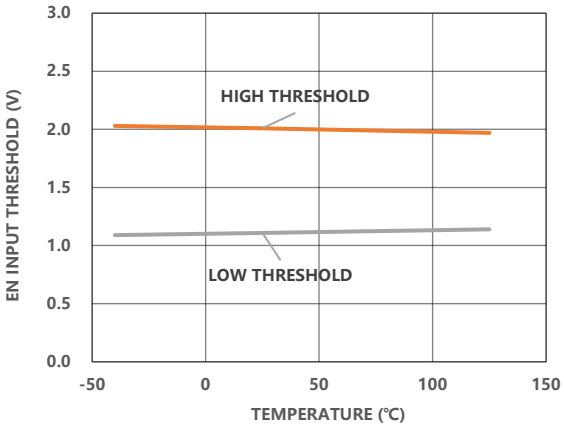


Figure 13 EN Input Threshold vs. Temperature

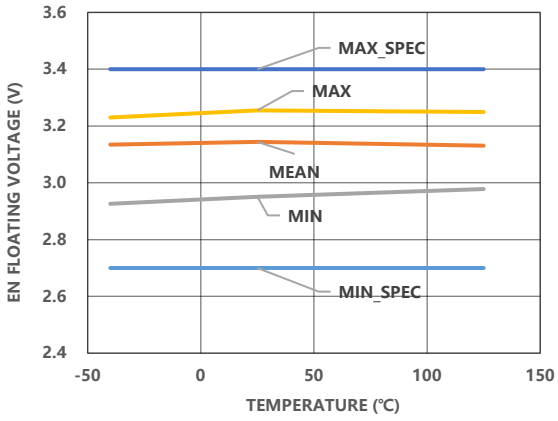


Figure 14 EN Floating Voltage vs. Temperature

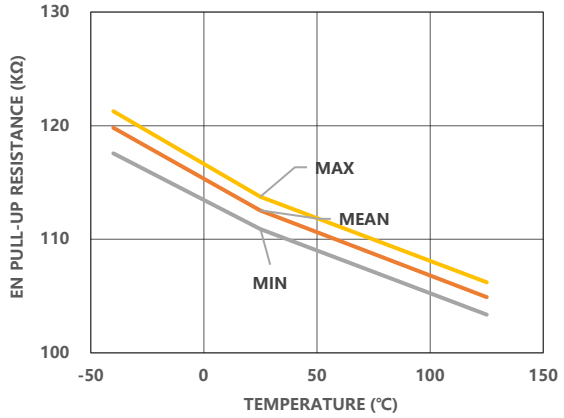


Figure 15 EN Pull-up Resistance vs. Temperature

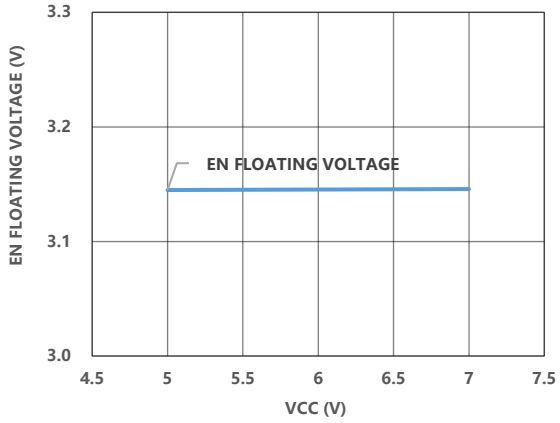


Figure 16 EN Floating Voltage vs. VCC

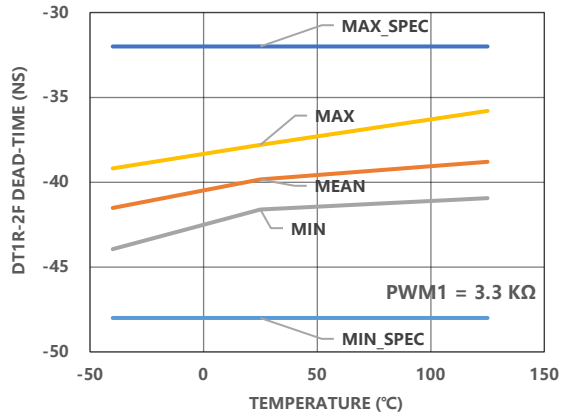


Figure 17 DT1R-2F Initial Dead-Time vs. Temperature, 3.3 kΩ Pull-down Resistor on the PWM1 (IR)

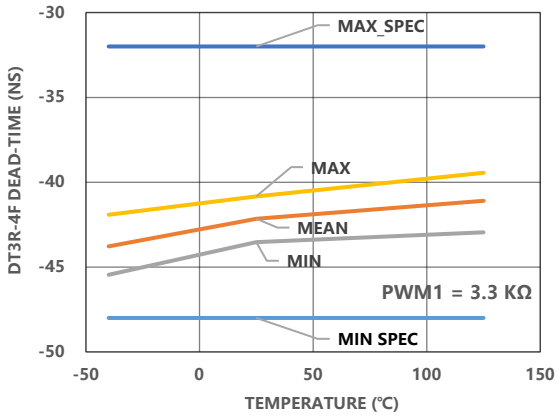


Figure 18 DT3R-4F Initial Dead-Time vs. Temperature, 3.3 kΩ Pull-down Resistor on the PWM1 (IR)

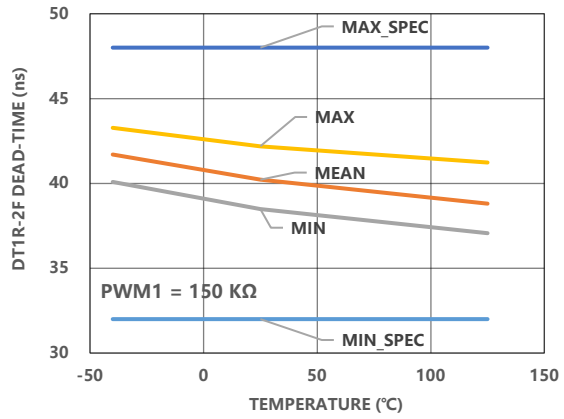


Figure 19 DT1R-2F Initial Dead-Time vs. Temperature, 150 kΩ Pull-down Resistor on the PWM1 (IR)

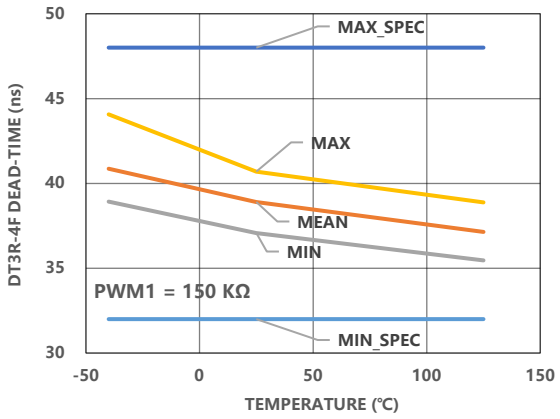


Figure 20 DT3R-4F Initial Dead-Time vs. Temperature, 150 kΩ Pull-down Resistor on the PWM1 (IR)

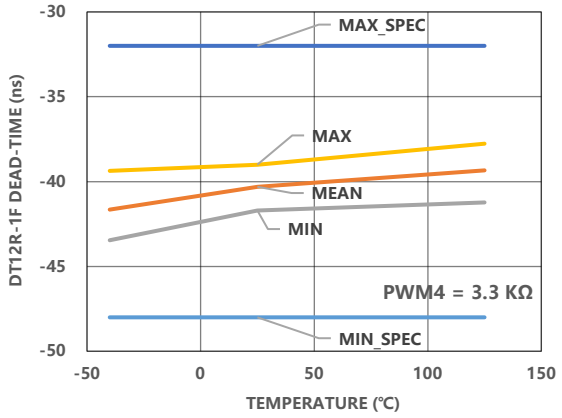


Figure 21 DT2R-1F Initial Dead-Time vs. Temperature, 3.3 kΩ Pull-down Resistor on the PWM4 (IF)

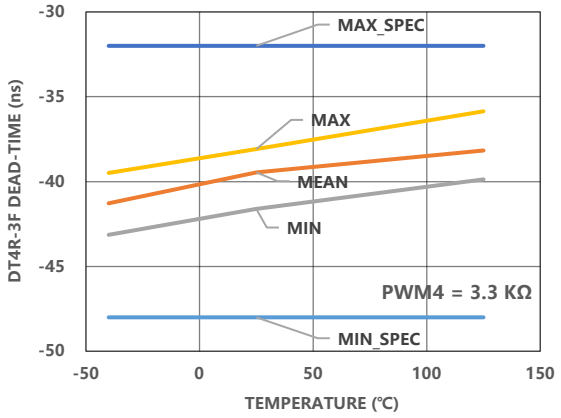


Figure 22 DT4R-3F Initial Dead-Time vs. Temperature, 3.3 kΩ Pull-down Resistor on the PWM4 (IF)

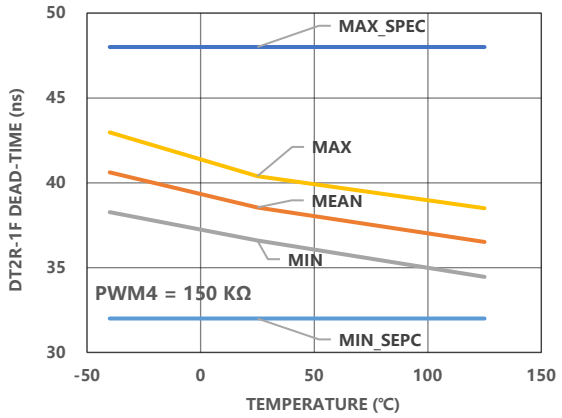


Figure 23 DT2R-1F Initial Dead-Time vs. Temperature, 150 kΩ Pull-down Resistor on the PWM4 (IF)

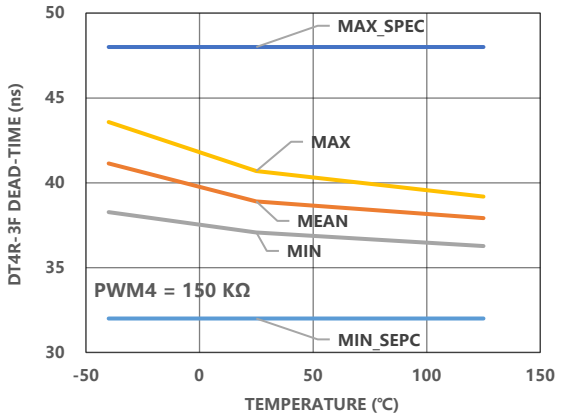


Figure 24 DT4R-3F Initial Dead-Time vs. Temperature, 150 kΩ Pull-down Resistor on the PWM4 (IF)

THEORY OF OPERATION

OVERVIEW

The OSU1800 is a phase multiplier IC designed to enhance multi-phase power systems by generating two complementary PWM pairs from a single PWM input, effectively doubling phase count. Targeting high-efficiency applications like desktop PCs and data centers, it integrates seamlessly with controllers, drivers, or power stages, enabling scalable power delivery.

Its compact DFN2x2-8L package, wide voltage range (5 V to 7 V), and industrial-grade temperature tolerance (-40°C to +125°C) ensure robust performance in space-constrained, high-density designs, bridging controller flexibility with power-stage optimization for next-generation computing infrastructure.

INPUT/OUTPUT PWM SIGNALS

The external PWM input is connected to PWM_IN. The internal partial frequency circuit generates two PWM channels, which are output through PWM1 and PWM3. Another two additional PWM channels are generated and output at PWM2 and PWM4. PWM2 provides the complementary signal to PWM1, and PWM4 provides the complementary signal to PWM3. When PWM_IN is within Tri-State window, the OSU1800 enters a Tri-State condition and the signals including PWM1, PWM2, PWM3 and PWM4 are driven to a low level.

PWM_IN must initiate a complete pulse on the PWM outputs before resuming normal operation from Tri-State condition as shown in Figure 25 and Figure 26. Prior to this initiation, the PWM output remains at a low level. It is crucial to avoid PWM output errors that may arise from incorrect dead-time configurations.

In the output sequence, PWM1 starts outputting first, followed by PWM3.

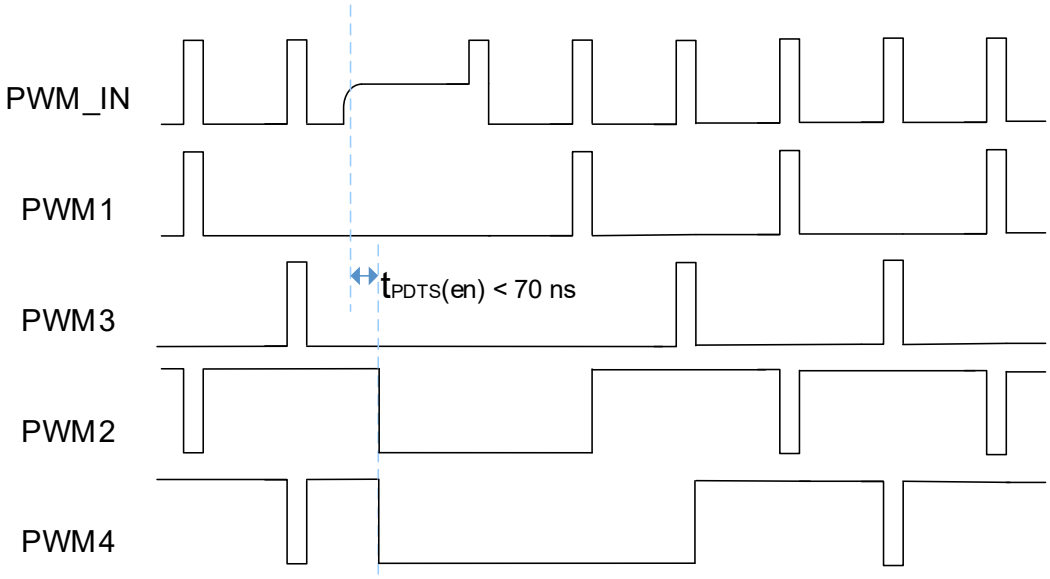


Figure 25 PWM Entering Tri-state Mode (a)

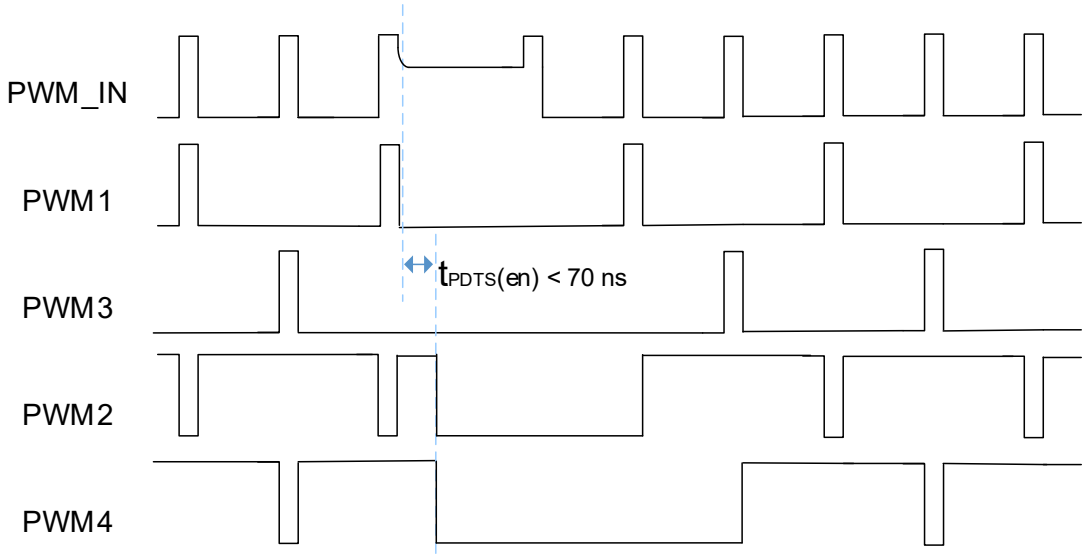


Figure 26 PWM Entering Tri-state Mode (b)

DT INITIALIZATION

The pull-down resistors on PWM1 and PWM4 determine the initial dead-time. Refer to the tables below for resistor-value-to-dead-time mappings. The delay time from PWM_IN to rising/falling edges of PWMx (x = 1 to 4) are defined as Figure 27 shown.

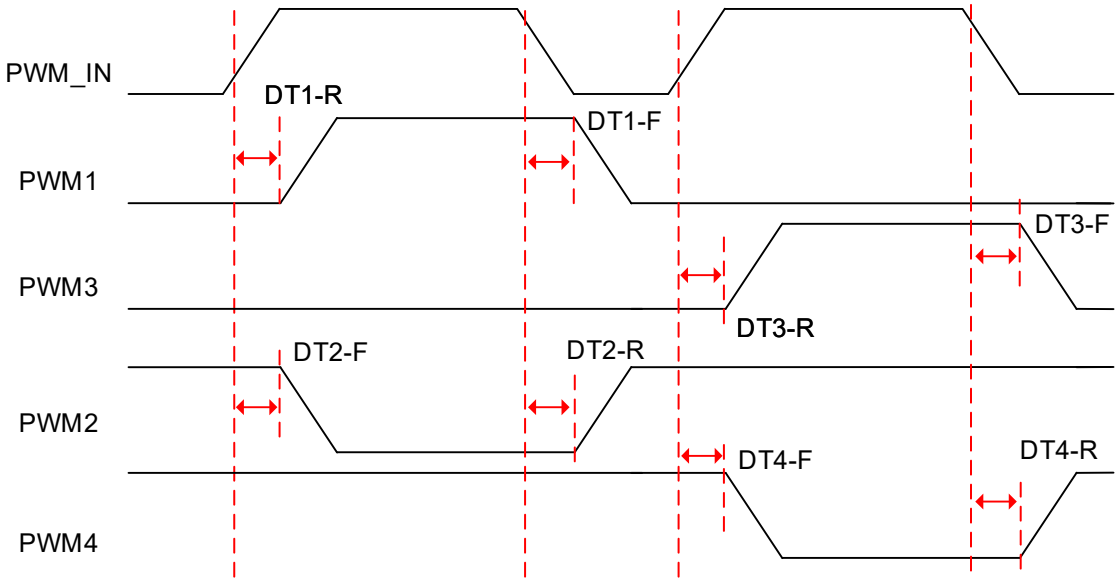


Figure 27 Timming Diagram of Dead Time

Table 5 PWM1 Pull Down Resistor

Resistor (kΩ)	DT1-R (ns)	DT3-R (ns)	DT2-F (ns)	DT4-F (ns)
3.3	40	40	80	80
4.7	44	44	76	76
6.8	48	48	72	72
10	52	52	68	68
15	56	56	64	64
22	60	60	60	60

33	64	64	56	56
47	68	68	52	52
68	72	72	48	48
100	76	76	44	44
150	80	80	40	40

Table 6 PWM4 Pull Down Resistor

Resistor (kΩ)	DT1-F (ns)	DT3-F (ns)	DT2-R (ns)	DT4-R (ns)
3.3	80	80	40	40
4.7	76	76	44	44
6.8	72	72	48	48
10	68	68	52	52
15	64	64	56	56
22	60	60	60	60
33	56	56	64	64
47	52	52	68	68
68	48	48	72	72
100	44	44	76	76
150	40	40	80	80

Table 9 DT Accuracy PWM1 (-40 to +125°C)

PWM1(IR) Resistor setting (kΩ)		Min	Typ	Max	Unit
3.3	(DT1-R) - (DT2-F)	-48	-40	-32	ns
4.7	(DT1-R) - (DT2-F)	-40	-32	-24	ns
6.8	(DT1-R) - (DT2-F)	-32	-24	-16	ns
10	(DT1-R) - (DT2-F)	-24	-16	-8	ns
15	(DT1-R) - (DT2-F)	-16	-8	0	ns
22	(DT1-R) - (DT2-F)	-8	0	8	ns
33	(DT1-R) - (DT2-F)	0	8	16	ns
47	(DT1-R) - (DT2-F)	8	16	24	ns
68	(DT1-R) - (DT2-F)	16	24	32	ns
100	(DT1-R) - (DT2-F)	24	32	40	ns
150	(DT1-R) - (DT2-F)	32	40	48	ns
3.3	(DT3-R) - (DT4-F)	-48	-40	-32	ns
4.7	(DT3-R) - (DT4-F)	-40	-32	-24	ns
6.8	(DT3-R) - (DT4-F)	-32	-24	-16	ns
10	(DT3-R) - (DT4-F)	-24	-16	-8	ns
15	(DT3-R) - (DT4-F)	-16	-8	0	ns
22	(DT3-R) - (DT4-F)	-8	0	8	ns
33	(DT3-R) - (DT4-F)	0	8	16	ns
47	(DT3-R) - (DT4-F)	8	16	24	ns
68	(DT3-R) - (DT4-F)	16	24	32	ns

100	(DT3-R) - (DT4-F)	24	32	40	ns
150	(DT3-R) - (DT4-F)	32	40	48	ns

Table 10 DT Accuracy PWM4 (-40 to +125°C)

PWM4(IF) Resistor setting (kΩ)	Min	Typ	Max	Unit
3.3	(DT2-R) - (DT1-F)	-48	-40	-32	ns
4.7	(DT2-R) - (DT1-F)	-40	-32	-24	ns
6.8	(DT2-R) - (DT1-F)	-32	-24	-16	ns
10	(DT2-R) - (DT1-F)	-24	-16	-8	ns
15	(DT2-R) - (DT1-F)	-16	-8	0	ns
22	(DT2-R) - (DT1-F)	-8	0	8	ns
33	(DT2-R) - (DT1-F)	0	8	16	ns
47	(DT2-R) - (DT1-F)	8	16	24	ns
68	(DT2-R) - (DT1-F)	16	24	32	ns
100	(DT2-R) - (DT1-F)	24	32	40	ns
150	(DT2-R) - (DT1-F)	32	40	48	ns
3.3	(DT4-R) - (DT3-F)	-48	-40	-32	ns
4.7	(DT4-R) - (DT3-F)	-40	-32	-24	ns
6.8	(DT4-R) - (DT3-F)	-32	-24	-16	ns
10	(DT4-R) - (DT3-F)	-24	-16	-8	ns
15	(DT4-R) - (DT3-F)	-16	-8	0	ns
22	(DT4-R) - (DT3-F)	-8	0	8	ns
33	(DT4-R) - (DT3-F)	0	8	16	ns
47	(DT4-R) - (DT3-F)	8	16	24	ns
68	(DT4-R) - (DT3-F)	16	24	32	ns
100	(DT4-R) - (DT3-F)	24	32	40	ns
150	(DT4-R) - (DT3-F)	32	40	48	ns

TYPICAL APPLICATION CIRCUITS

Figure 28 demonstrates a typical application circuit of the OSU1800 for driving an interleaved half-bridge current doubler converter. This converter steps down the input voltage from typically 48 V to 1.2 V using only single power stage, increasing the power conversion efficiency comparing to two stage conversion. PWM_IN and EN are controlled by an external multi-phase controller. The PWM1-PWM4 outputs drive both the half-bridge driver HP3010 (120 V/ 3 A) and the dual-channel low-side driver HP3000 (30 V/ 5 A). Initial dead times between complementary pairs (PWM1/PWM2 and PWM3/PWM4) are independently configured via resistors R_1 at PWM1 and R_4 at PWM4.

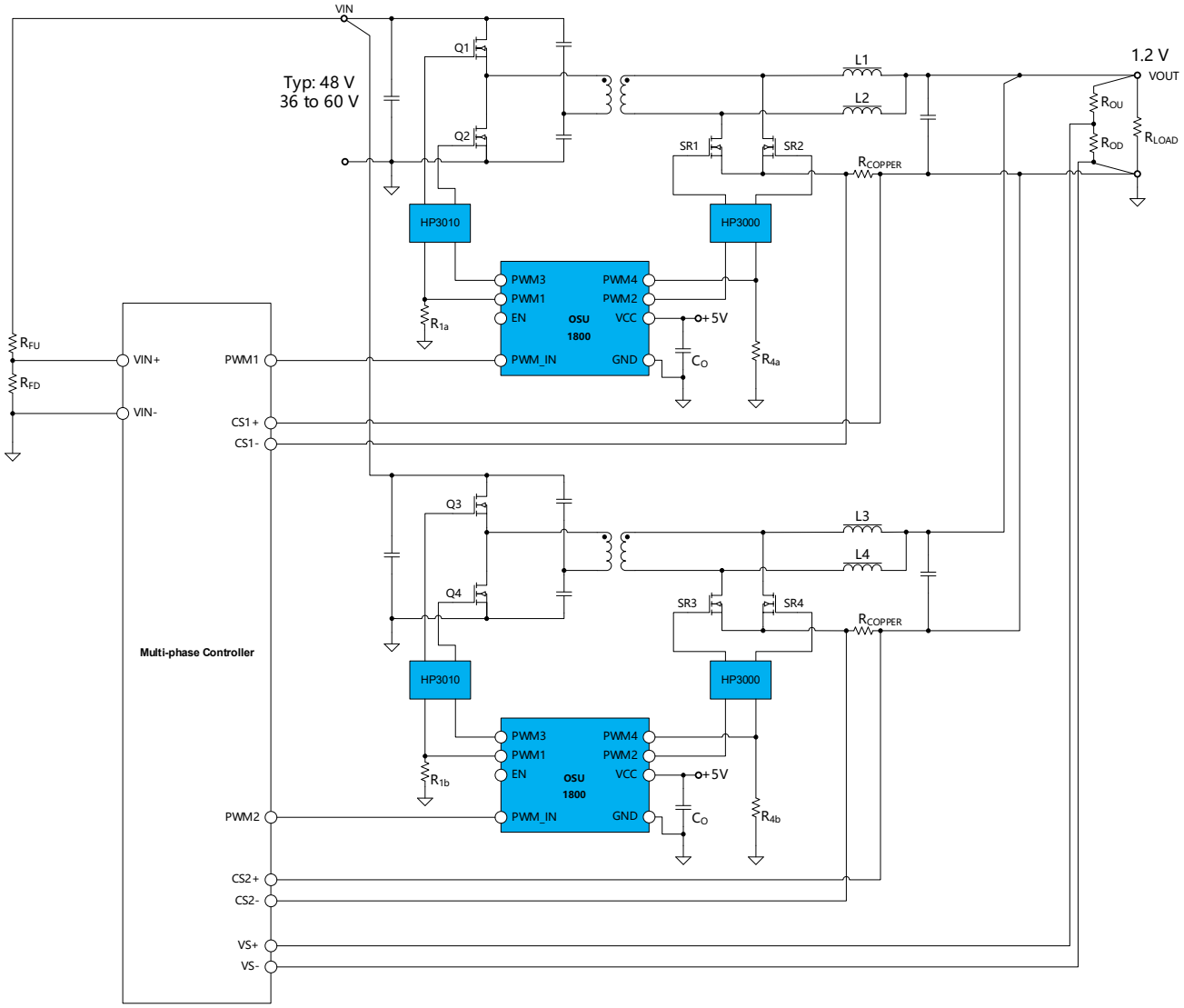
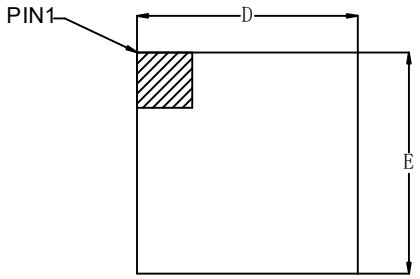
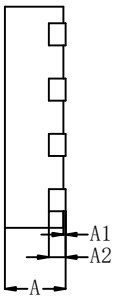


Figure 28 Typical Application Circuit

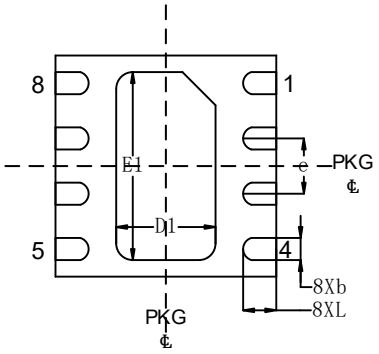
PACKAGE OUTLINE DIMENSIONS



TOP VIEW



SIDE VIEW



	DIMENSION IN MILLIMETERS		
SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.152 REF	
b	0.15	0.20	0.25
D		2 BSC	
E		2 BSC	
e		0.5 BSC	
L	0.25	0.30	0.35
D1	0.80	0.90	1.00
E1	1.60	1.70	1.80

Figure 29 OSU1800-AA000-DN08R Dimensions

PACKAGE TOP MARKING

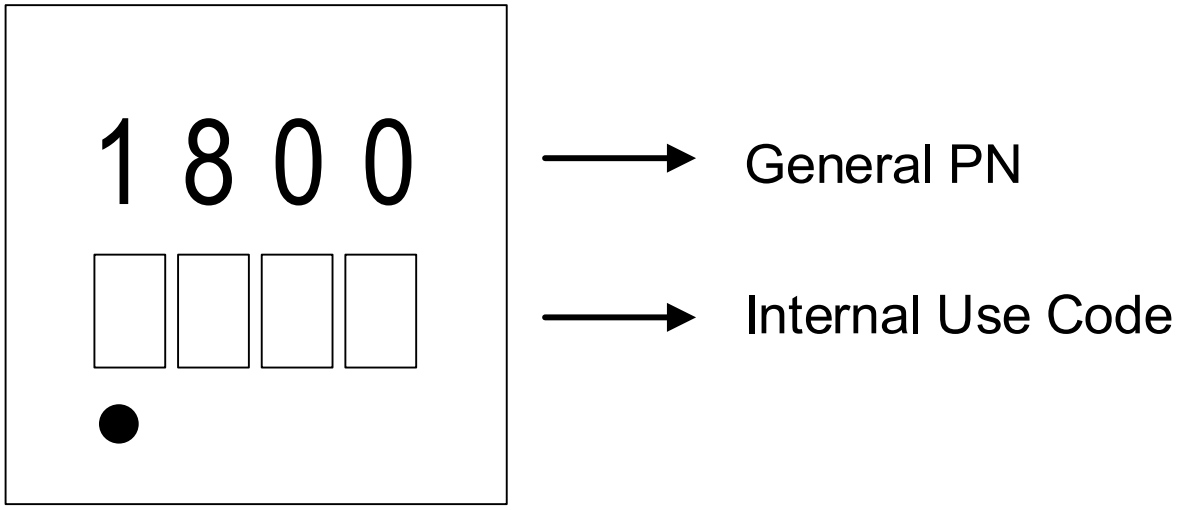
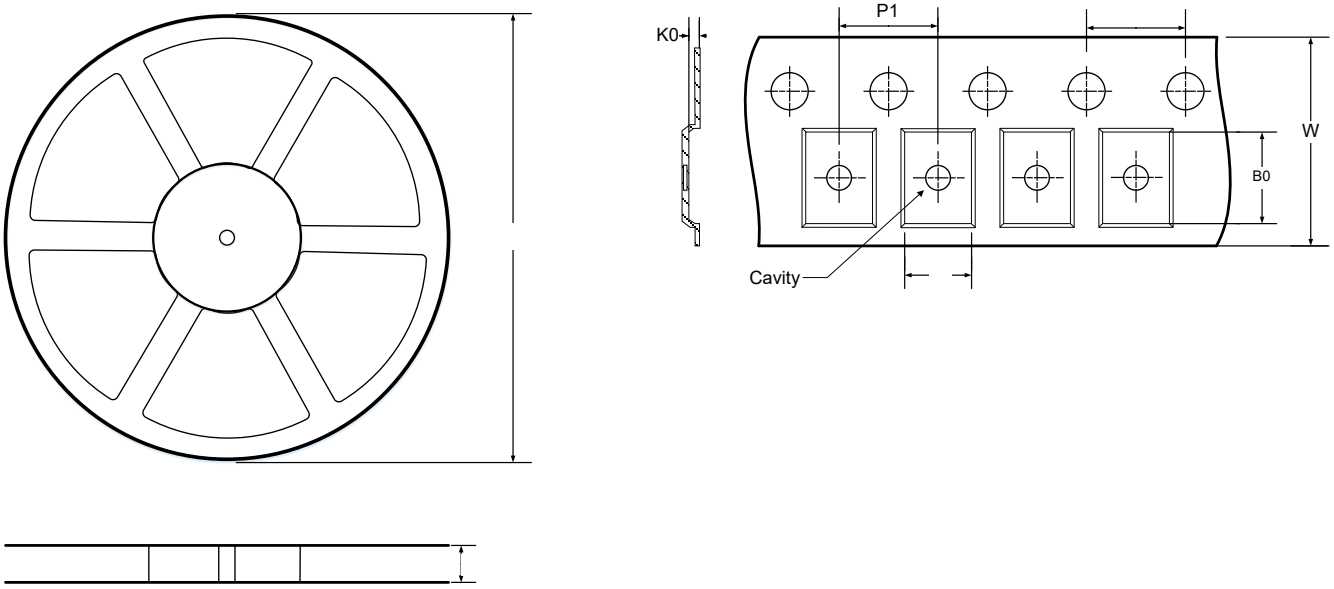


Figure 30 OSU1800-AA000-DN08R Package Top Marking

ORDERING GUIDE

Model	Temperature Range	Package Type	MSL	Package Option	Quantity
OSU1800-AA000-DN08R	-40°C to +125°C	DFN2x2-8L	1	T&R	4000

TAPE AND REEL INFORMATION



DIMENSIONS AND PIN1 ORIENTATION

D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180.00	9.50	2.20	2.20	0.75	4.00	4.00	8.00	Q2

All dimensions are nominal

Figure 31 Tape and Reel Information

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