General Description

OSNE65R065TD1 is an enhancement mode GaN-on-Si power transistor. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The TO-Leadless package offers low parasitic resistance/inductance, strong heat dissipation and high solderability, releasing device potential and make GaN better apply to industrial applications.

Features

- 650V GaN enhancement-mode power switch
- Ultra fast switching
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- RoHS, Pb-free, REACH-compliant

RoHS compliant

Applications

- LED lighting drivers
- Bridgeless totem pole PFC
- High frequency LLC
- Solar inverters, energy storage systems
- Consumer, industrial and datacenter high density power supply
- Appliance and industrial motor drives

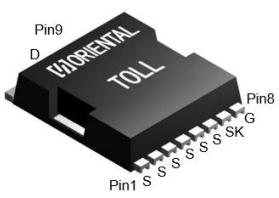
Key Performance Parameters (T_{case}=25℃ except as noted)

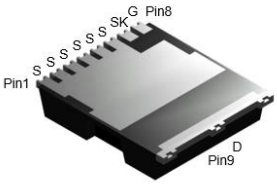
Parameter	Value	Unit
V_{DS}	650	V
$I_{D,\ pulse}$	60	A
$R_{DS(ON),\ max}$ @V_{GS}=6 V	65	mΩ
Q_g	6.5	nC

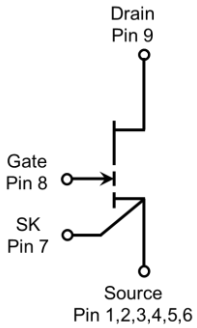
Marking Information

Product Name	Package	Marking
OSNE65R065TD1	TOLL	OSNE65R065TD1

Package & Pin Information







Absolute Maximum Ratings at Tj=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Drain-source voltage transient [1]	$V_{DS,\ transient}$	850	V
Gate to source voltage, continuous[2], T_j=-55 °C to 150 °C	V_{GS}	-7/+7	V
Gate to source voltage, pulsed[3], T_j=-55 °C to 150 °C	$V_{GS,\ pulse}$	-20/+10	V
Continuous drain current	I_D	30	A
Pulsed drain current [4]	$I_{D,\ pulse}$	60	A
Pulsed drain current [4], T_j=150 °C	$I_{D,\ pulse}$	25	A
Power dissipation	P_{tot}	169	W
Operation temperature	T_j	-55 to 150	°C
Storage temperature	T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.74	°C/W
Thermal resistance, junction-ambient [5]	$R_{\theta JA}$	40	°C/W
Reflow soldering temperature	T_{sold}	260	°C

Static Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS}=V_{GS}, I_D=7.5 mA
			1.9			V_{DS}=V_{GS}, I_D=7.5 mA, T_j=150 °C
Drain-source on-state resistance	$R_{DS(ON)}$		50	65	mΩ	V_{GS}=6 V, I_D=15 A
			120			V_{GS}=6 V, I_D=15 A, T_j=150 °C
Gate-source leakage current	I_{GSS}		160		μA	V_{GS}=6 V, V_{DS}=0 V
Drain-source leakage current	I_{DSS}		2	55	μA	V_{DS}=650 V, V_{GS}=0 V
			105			V_{DS}=650 V, V_{GS}=0 V, T_j=150 °C
Gate resistance	R_G		1.6		Ω	f=5 MHz, Open drain

Dynamic Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		225		pF	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Output capacitance	C_{oss}		60		pF	
Reverse transfer capacitance	C_{rss}		0.8		pF	
Effective output capacitance, energy related	$C_{o(er)}$		102		pF	V_{GS}=0 V, V_{DS}=0 V-400 V
Effective output capacitance, time related	$C_{o(tr)}$		151		pF	
Turn on delay time	$t_{d(on)}$		8.2		ns	V_{GS}=6 V, V_{DS}=400 V, R_{on}=10 Ω, R_{off}=1 Ω, I_D=15 A, L=100 μH
Rise time	t_r		5.5		ns	
Turn off delay time	$t_{d(off)}$		9.8		ns	
Fall time	t_f		5.4		ns	
Output Charge	Q_{oss}		60		nC	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Output Capacitance Stored Energy	E_{oss}		8.2		μJ	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		6.3		nC	V_{GS}=6 V, V_{DS}=400 V, I_D=30 A
Gate-source charge	Q_{gs}		1.6		nC	
Gate-drain charge	Q_{gd}		1.9		nC	

Reverse conduction characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Source-drain reverse voltage	V_{SD}		2.9		V	I_S=30 A, V_{GS}=0 V
Pulsed current, reverse	$I_{S,\ pulse}$		50		A	V_{GS}=6 V
Reverse recovery time	t_{rr}		0		ns	I_S=30 A, V_R=400 V
Peak reverse recovery current	I_{rrm}		0		A	
Reverse recovery charge	Q_{rr}		0		nC	

Notes

1. $V_{DS,\ transient}$ is intended for surge rating during non-repetitive events, t_{Pulse}<1 μs.
2. The minimum V_{GS} is clamped by ESD protection circuit.
3. Pulse width =50 ns, f=100 kHz.
4. Pulse width =10 us.
5. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.889 mm pitch (35 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Electrical Characteristics Diagrams

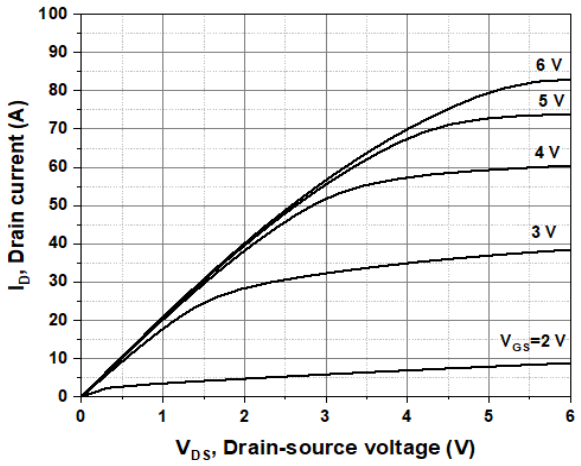


Figure 1. Typ. output characteristics T_j=25 ℃

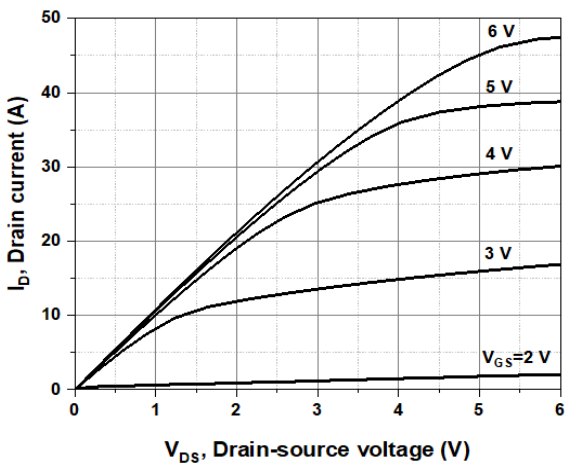


Figure 2. Typ. output characteristics T_j=150 ℃

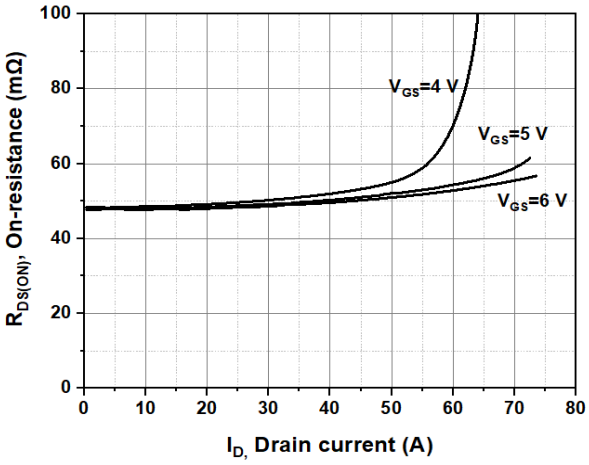


Figure 3. Typ. on-resistance vs. drain current for T_j=25 ℃

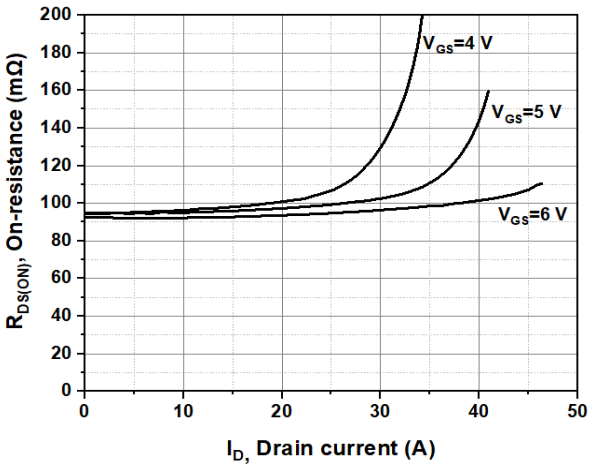


Figure 4. Typ. on-resistance vs. drain current for T_j=150 ℃

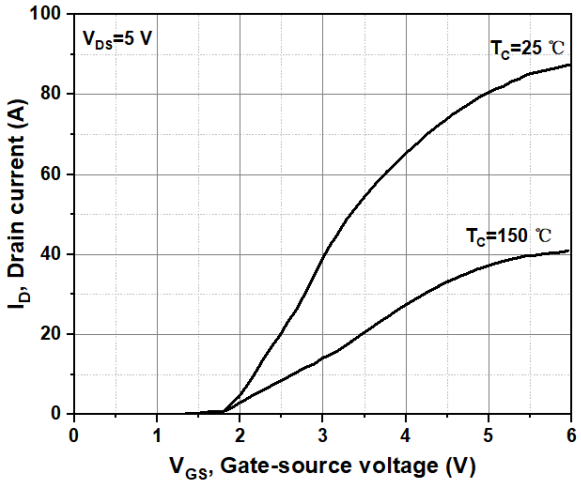


Figure 5. Typ. transfer characteristic for various case temperatures

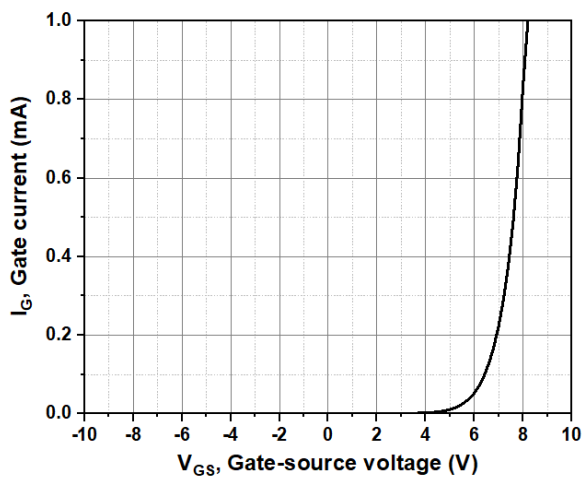


Figure 6. Typ. Gate-Source leakage characteristics

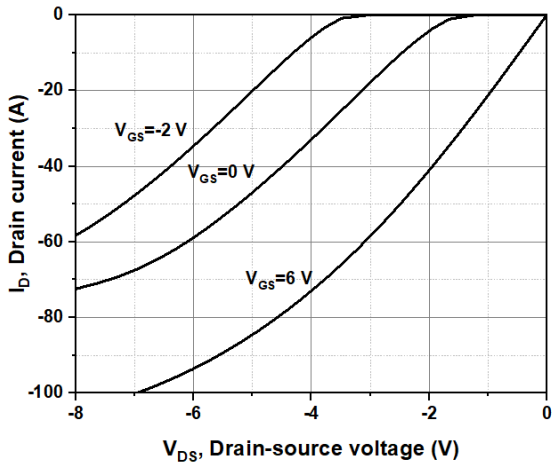


Figure 7. Channel reverse characteristics at T_j=25 ºC

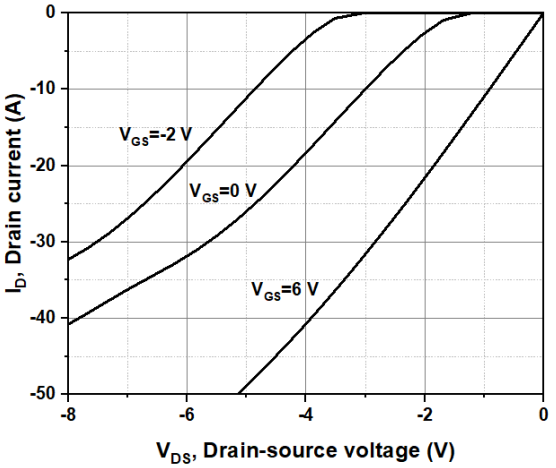


Figure 8. Channel reverse characteristics at T_j=150 ºC

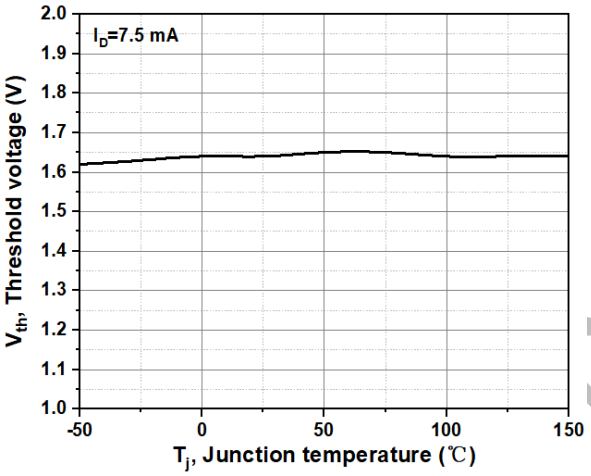


Figure 9. Threshold voltage vs. temperature, V_{GS}=V_{DS}, I_D=7.5 mA

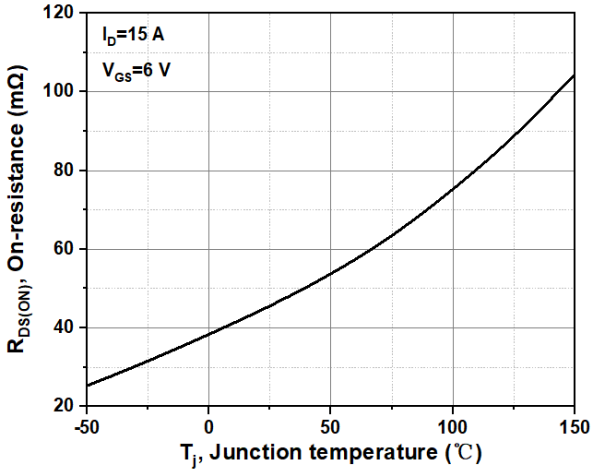


Figure 10. Drain-source on-state resistance vs. temperature, I_D=15 A, V_{GS}=6 V

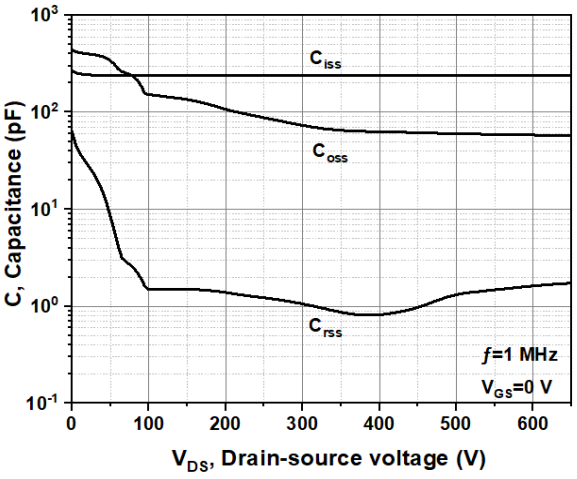


Figure 11. Capacitances vs. drain-source voltage

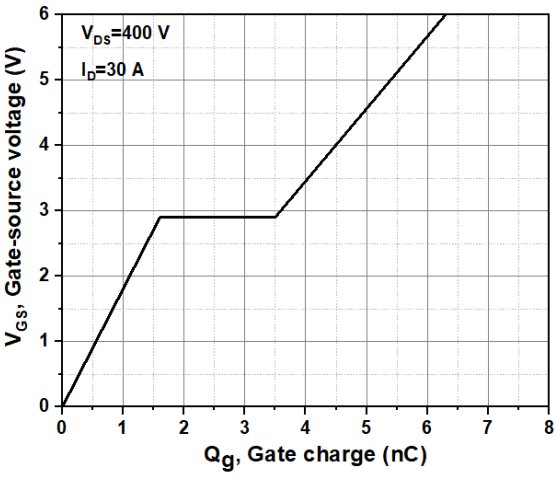


Figure 12. Gate charge characteristic

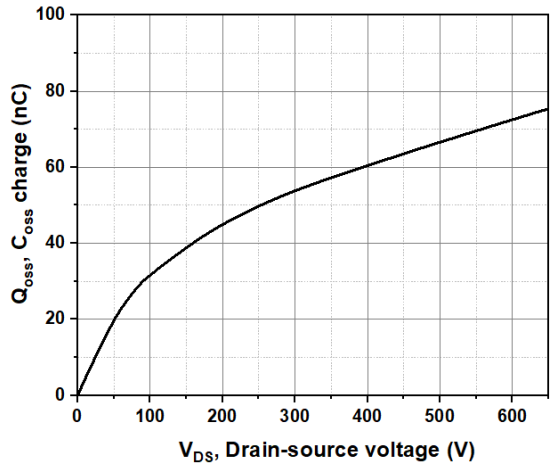


Figure 13. Typ. output charge, Freq=1 MHz.

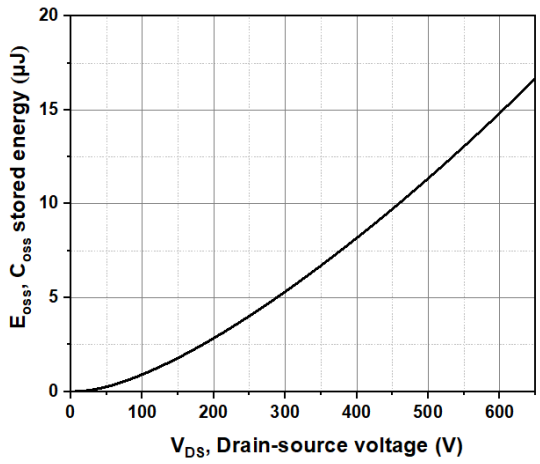


Figure 14. Typ. C_{oss} stored energy, Freq=1 MHz

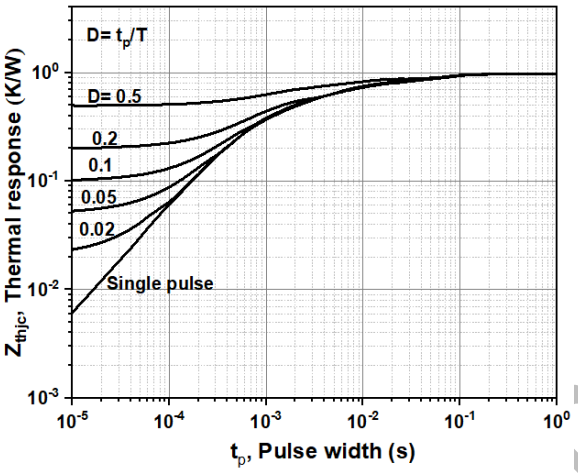


Figure 15. Transient thermal impedance (junction-case)

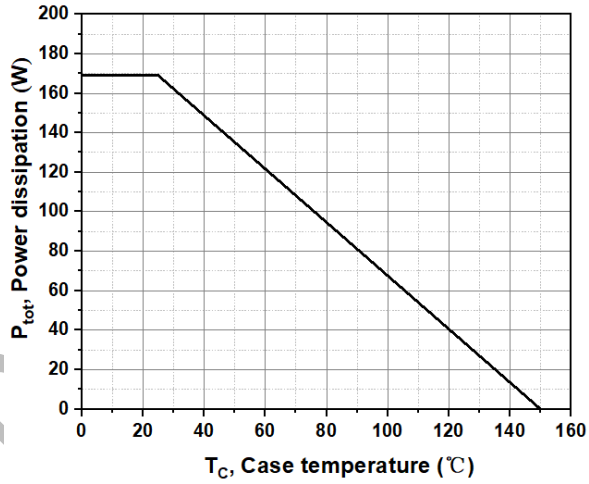


Figure 16. Maximum power dissipation derating vs. case temperature

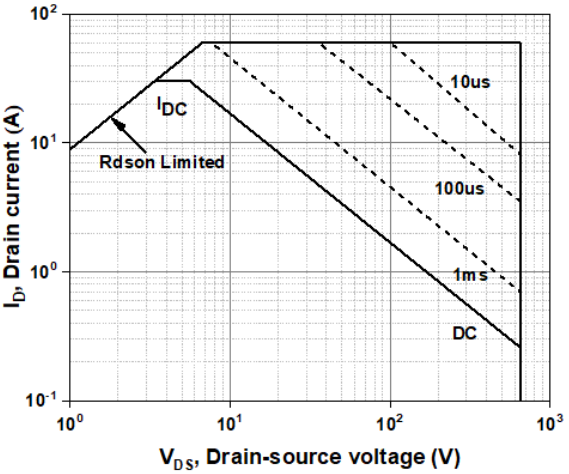


Figure 17. Safe operating area

Test circuits and waveforms

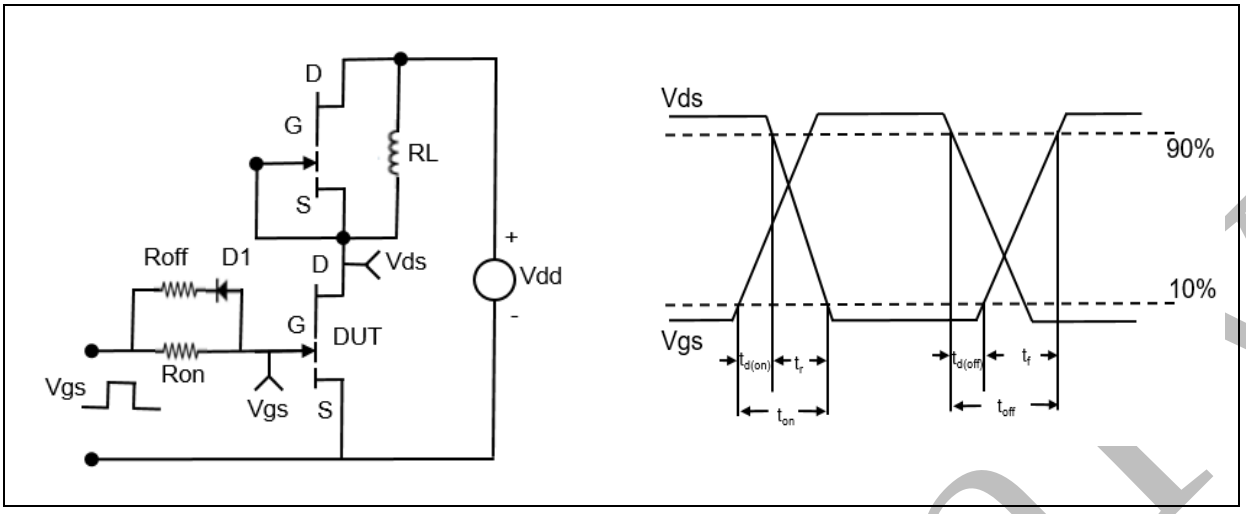
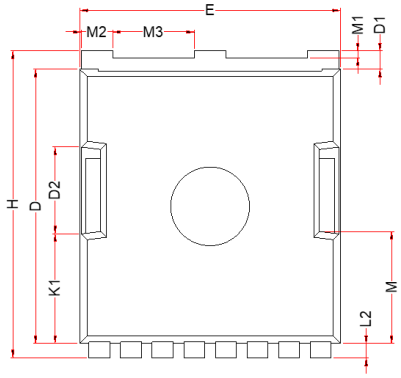
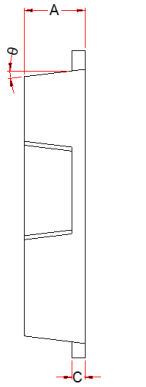
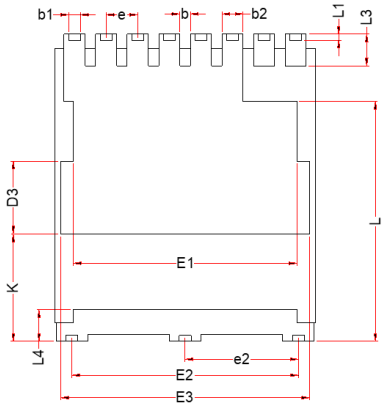


Figure 1. Switching time test circuit & waveforms

Package Information







Symbol	mm	
	Min	Max
A	2.20	2.40
b	0.30	0.50
b1	0.35	0.55
b2	0.70	0.90
c	0.40	0.60
D	10.28	10.58
D1	0.60	0.80
D2	(3.30)	
D3	(2.77)	
E	9.70	10.10
E1	(8.50)	
E2	(8.50)	
E3	(9.46)	
e	1.10	1.30
H	11.48	11.88
K	(4.08)	
K1	(4.17)	
L	(9.13)	
L1	0.13	0.33
L2	0.50	0.70
L3	1.10	1.30
L4	1.10	1.30
M	(4.23)	
M1	0.16	0.36
M2	1.10	1.30
M3	3.00	3.20
θ	4°	10°
e2	4.20	4.40

Version: TOLL package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TOLL	2000	1	2000	7	14000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
OSNE65R065TD1	TOLL	yes	yes	yes

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